Pioneer

Service Manual

SERVICE GUIDE

ORDER NO.
RRV2055

COMPACT DISC RECORDER

PDR-555RW
PDR-V500
PDR-19RW
PDR-509

PIONEER CORPORATION 4-1, Meguro 1-chome, Meguro-ku, Tokyo 153-8654, Japan
PIONEER ELECTRONICS SERVICE, INC. P.O. Box 1760, Long Beach, CA 90801-1760, U.S.A.
PIONEER ELECTRONIC (EUROPE) N.V. Haven 1087, Keetberglaan 1, 9120 Melsele, Belgium
PIONEER ELECTRONICS ASIACENTRE PTE. LTD. 253 Alexandra Road, #04-01, Singapore 159936
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CONTENTS

1. BLOCK DIAGRAM 4
1.1 PDR-555RW, PDR-V500 AND PDR-19RW 4
1.2 PDR-509 6

2. PRODUCT DESCRIPTIONS 8

3. PORT TABLE OF MICROCOMPUTER 9
3.1 MODE CONTROL OF PDR-555RW, PDR-V500 AND PDR-19RW 9
3.2 MECHANISM CONTROL OF PDR-555RW, PDR-V500 AND PDR-19RW 11
3.3 MODE CONTROL OF PDR-509 14
3.4 MECHANISM CONTROL OF PDR-509 16

4. PIN FUNCTION OF PRINCIPAL IC 19
4.1 AD1893JST 19
4.2 BR93LC46AF 19
4.3 LC89585 20
4.4 LH64256CK-70 22
4.5 PA9004A 22
4.6 PDJ014A 23
4.7 PDK033A or PDK041A 24
4.8 AK5340-VS 25
4.9 PD0236AD 26
4.10 PCM1800-1 26

5. RECORDING MECHANISM FOR CD-Rs AND CD-RWs 27
5.1 DISC 27
5.2 OVERWRITE RECORDING OF CD-RW 27

6. PICKUP (KRS-200A) 28

7. CIRCUIT DESCRIPTIONS 29
7.1 SERVO CIRCUITS 29
7.1.1 Control Circuit for the Laser Diode 29
7.1.2 Error Signal Generation Circuit 29
7.1.3 Focus Servo 29
7.1.4 Tracking Thread Servo 29
7.1.5 Spindle Servo 29
7.2 DEFECT CIRCUIT 30
7.3 EFM-DIGITAL PLL 30
7.4 RF DETECTION 30
7.5 MIRROR CIRCUIT 30
7.6 AUDIO CIRCUITS 30
7.6.1 Analog Audio Input 30
7.6.2 A/D Converter 30
7.6.3 Hi-bit IC (PDR-19RW Only) 31
7.6.4 D/A Converter 31
7.6.5 Analog Audio Output Block 31
7.7 DIGITAL CIRCUITS 31
7.7.1 Digital Audio Interface Input Block 31
7.7.2 Sampling Rate Converter 31
7.7.3 Clock-jitter Suppressor Circuit (PDR-509 Only) 31
7.7.4 Data Selector 31
7.7.5 Digital Fader, Level Meter, Mute Blocks 31
7.7.6 Memory Control 31
7.7.7 EFM Encoding 32
7.7.8 Strategy Control 32
7.7.9 Digital Audio Interface Modulation 32

8. DETAILED DESCRIPTIONS OF OUTPUT TERMINAL CONTROL 32
8.1 DGAI (microcomputer,pin 48)and D8CM (microcomputer,pin 53)TERMINAL CONTROL 32
8.2 AGCON (ATIP decoder, pin 52) TERMINAL CONTROL 32
8.3 XCD (ATIP decoder, pin 69) TERMINAL CONTROL 33
8.4 GAINUP1 (ATIP decoder, pin 45) RW/XR (ATIP decoder, pin 66) TERMINAL CONTROL ... 33
8.5 CDROPC (ATIP decoder, pin 46) TERMINAL CONTROL 33
8.6 GAINUP3 (ATIP decoder, pin 47) TERMINAL CONTROL 33
8.7 PHYERS (ATIP decoder, pin 52) TERMINAL CONTROL 33
8.8 SSEL (ATIP decoder, pin 51) TERMINAL CONTROL 33
8.9 ENBL (ATIP decoder, pin 70) TERMINAL CONTROL 33

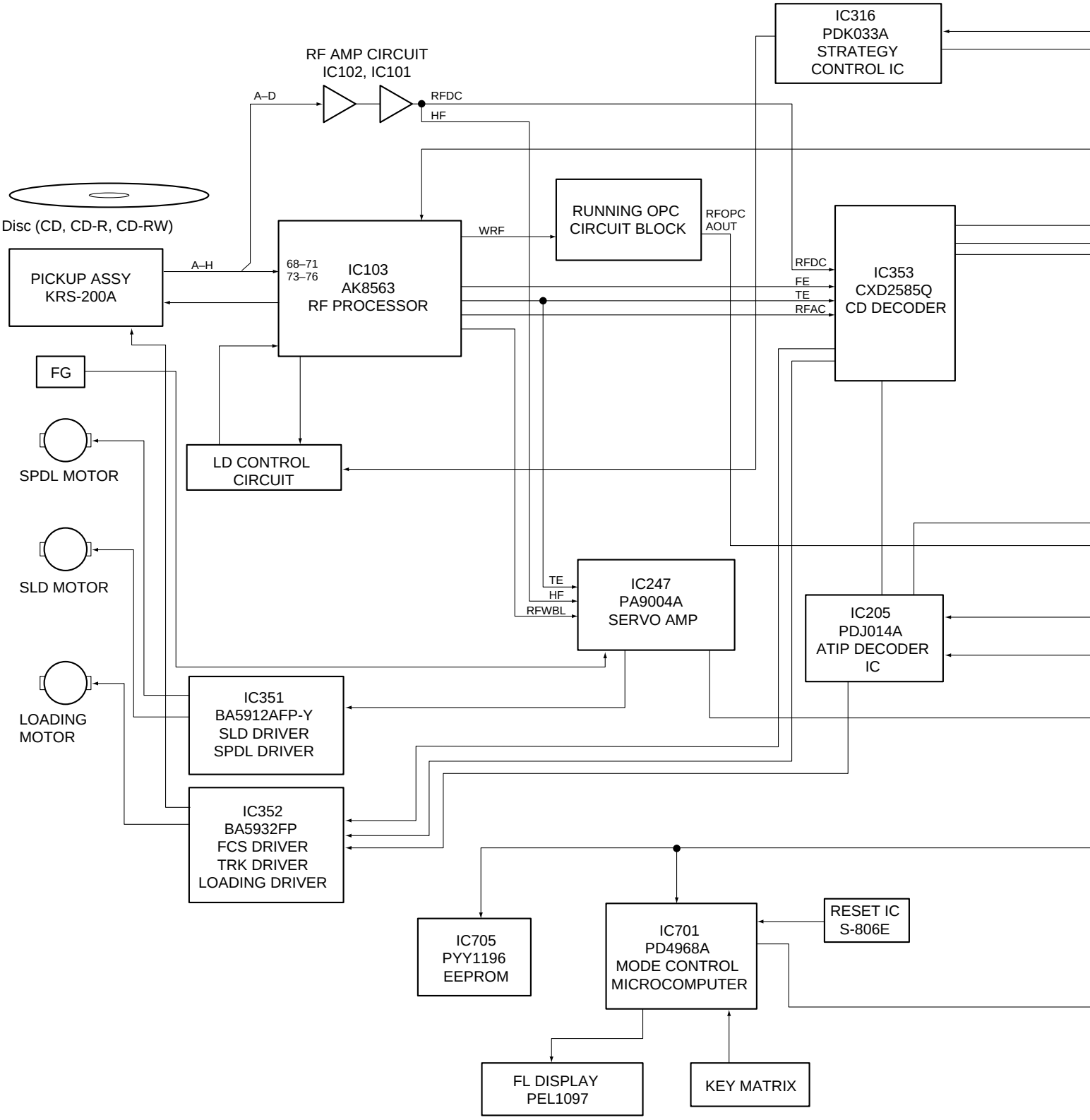
9. OPERATION DESCRIPTIONS 34
9.1 ABOUT POWER ON/OFF 34
9.1.1 Power-up (When the power outlet is active) 34
9.1.2 Power Down (When the power outlet is not active or power failure occurs) 34
9.2 ABOUT SERVO CONTROL 34
9.2.1 Seek Track 0 34
9.2.2 Focus ON 34
9.2.3 One-Track Jump (Direct Sequence) 35
9.2.4 One-Track Jump (Auto Sequence) 35
9.2.5 Ten-Track Jump 35
9.2.6 2N-Track Jump 35
9.2.7 M-Track Move 36
9.2.8 Fine Search 36
9.2.9 Loading Control 36
9.2.10 Spindle Control 37
9.3 ERASING (CD-RW ONLY) 37
9.3.1 Last-Track-Erase Operation 37
9.3.2 All-Track-Erase Operation 37
9.3.3 TOC-Erase Operation 37
9.3.4 ALL-Disc-Erase Operation 37
9.3.5 PCA-Erase Operation 37
9.4 RID CODES 37
9.5 DISC JUDGMENT 38
9.5.1 Tentative Judgment Using FZC (Distinguishing Between CD/CD-R and CD-RW) 38
9.5.2 Disc Judgment with Each Type of Disc 38
9.6 SETUP (FLOW) 39
9.6.1 Verification of Disc Judgments 40
9.6.2 Auto-Adjustments 40
9.6.3 Tracking Error Level Adjustment and Disc Determination 40
9.6.4 Recording Power Sweep Mode for Recording Power Calibration 41
9.6.5 Playback RF Estimating Mode for Recording Power Calibration 41

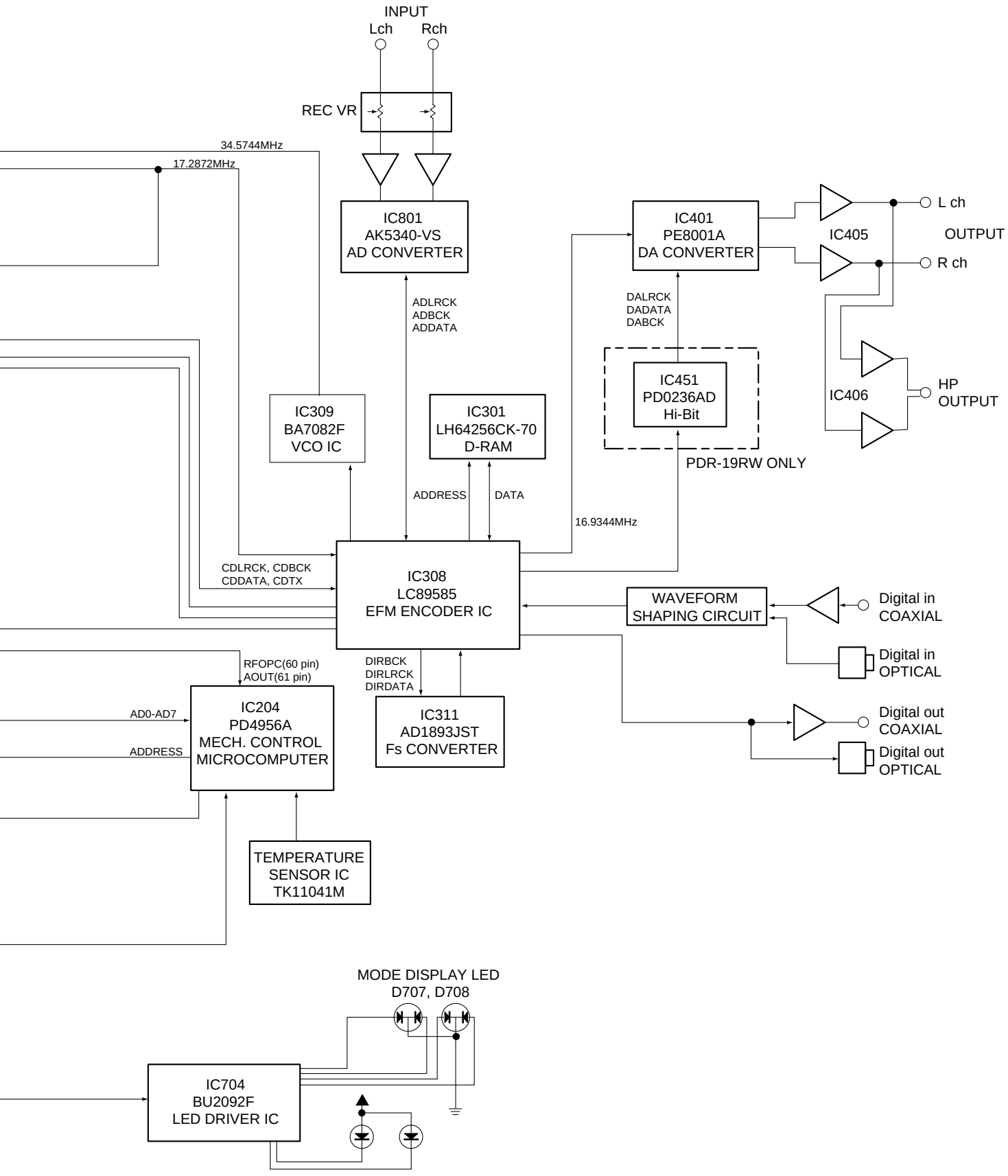
10. ABOUT TEST MODE OPERATIONS 41

11. ERROR CODES 45
11.1 ERROR CODE DISPLAY FOR SERVICE 45
11.2 ABOUT FULL ERROR CODES 47

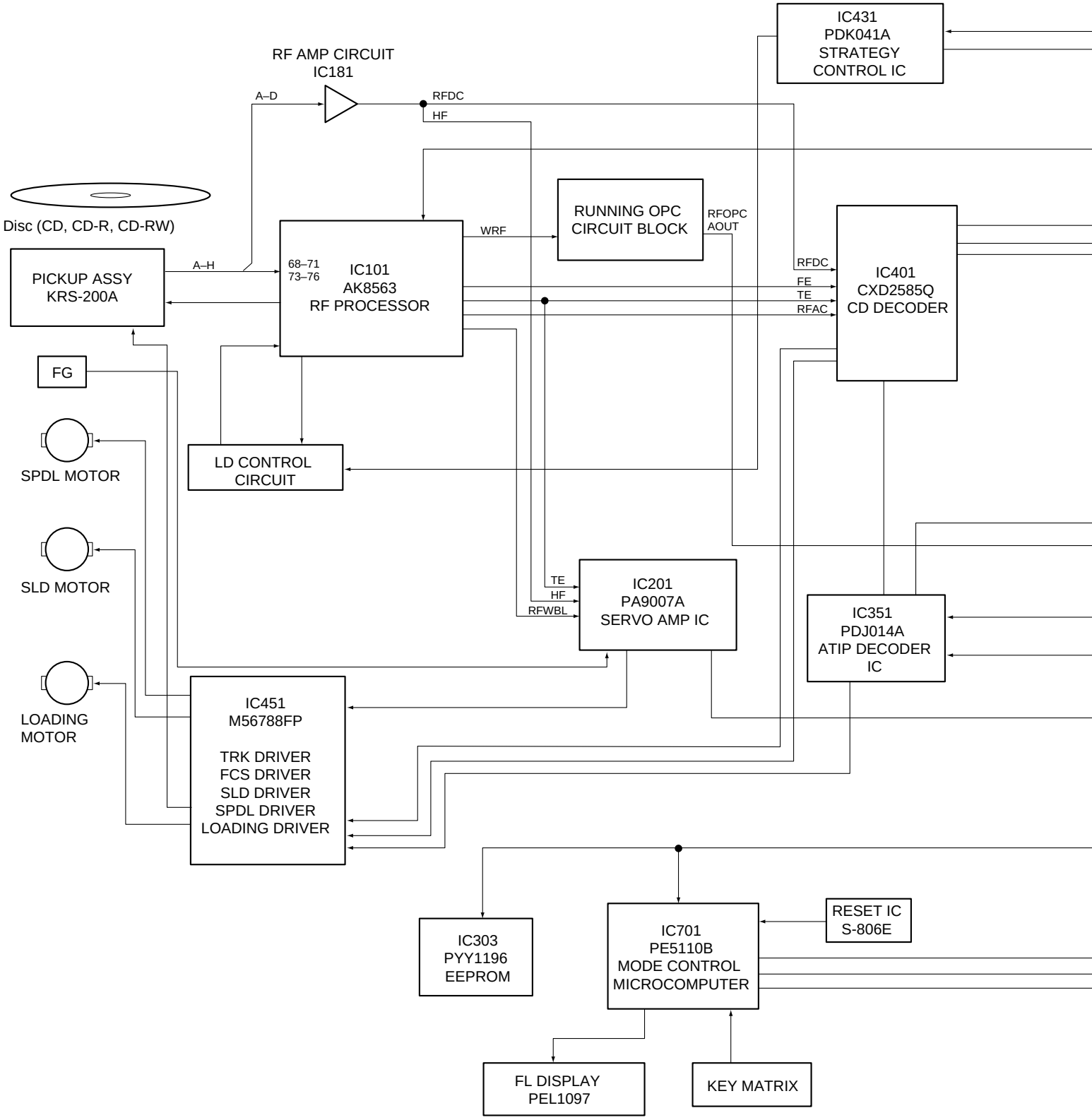
1. BLOCK DIAGRAM

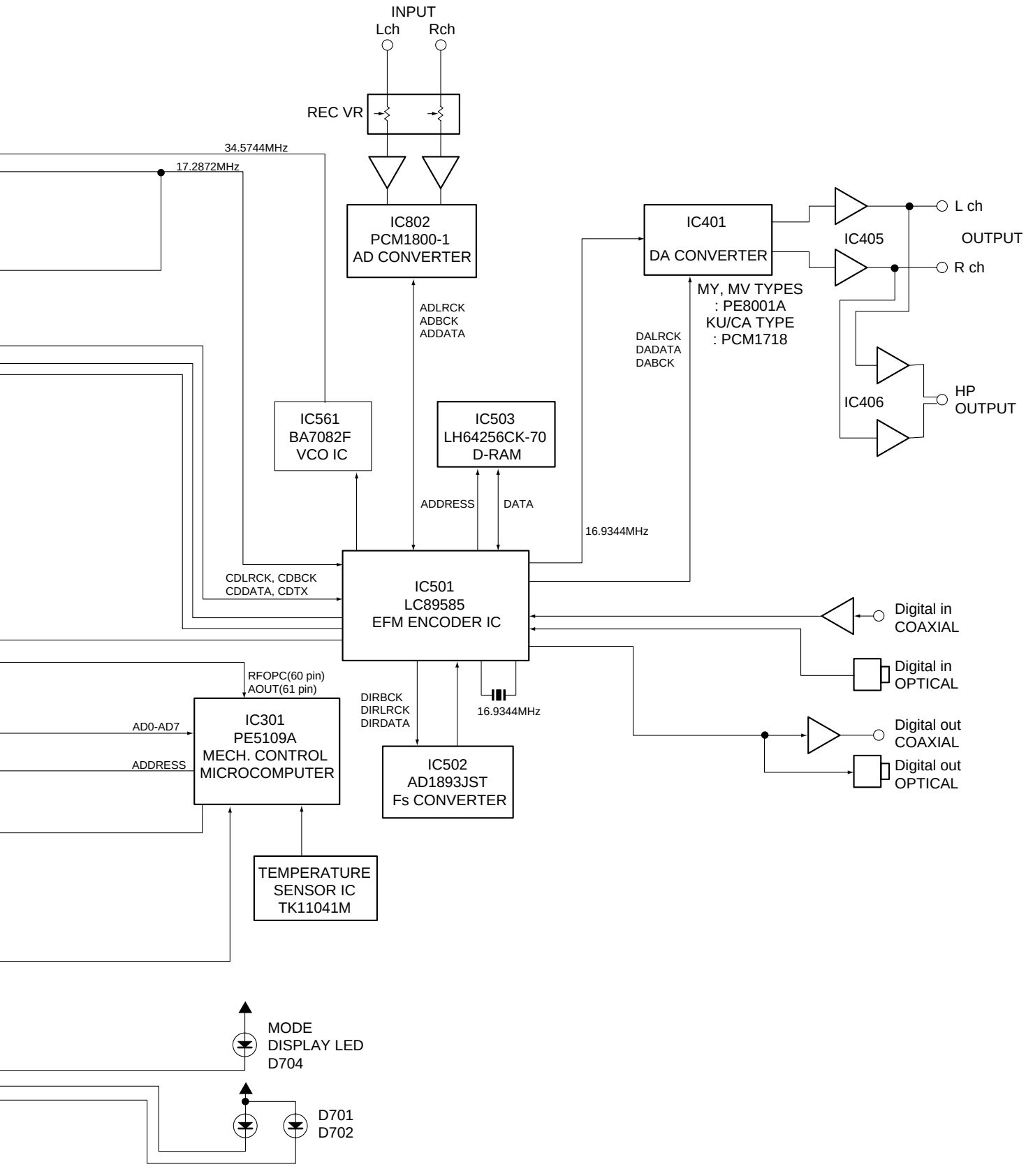
1.1 PDR-555RW, PDR-V500 AND PDR-19RW




INPUT
Lch
Rch
REC VR
34.5744MHz
17.2872MHz
IC801
AK5340-VS
AD CONVERTER
ADLRCK
ADBCK
ADDATA
IC401
PE8001A
DA CONVERTER
IC405
L ch
OUTPUT
R ch
DALRCK
DADATA
DABCK
IC451
PD0236AD
Hi-Bit
PDR-19RW ONLY
IC406
HP
OUTPUT
IC309
BA7082F
VCO IC
IC301
LH64256CK-70
D-RAM
ADDRESS
DATA
16.9344MHz
CDLRCK, CDBCK
CDDATA, CDTX
IC308
LC89585
EFM ENCODER IC
WAVEFORM
SHAPING CIRCUIT
Digital in
COAXIAL
Digital in
OPTICAL
RFOPC(60 pin)
AOUT(61 pin)
DIRBCK
DIRLRCK
DIRDATA
AD0-AD7
ADDRESS
IC204
PD4956A
MECH. CONTROL
MICROCOMPUTER
IC311
AD1893JST
Fs CONVERTER
Digital out
COAXIAL
Digital out
OPTICAL
TEMPERATURE
SENSOR IC
TK11041M
MODE DISPLAY LED
D707, D708
IC704
BU2092F
LED DRIVER IC

1.2 PDR-509


IC431
PDK041A
STRATEGY
CONTROL IC
RF AMP CIRCUIT
IC181
A–D
RFDC
HF
Disc (CD, CD-R, CD-RW)
RUNNING OPC
CIRCUIT BLOCK
RFOPC
AOUT
WRF
PICKUP ASSY
KRS-200A
A–H
68–71
73–76
IC101
AK8563
RF PROCESSOR
RFDC
FE
TE
RFAC
IC401
CXD2585Q
CD DECODER
FG
SPDL MOTOR
LD CONTROL
CIRCUIT
SLD MOTOR
TE
HF
RFWBL
IC201
PA9007A
SERVO AMP IC
IC351
PDJ014A
ATIP DECODER
IC
LOADING
MOTOR
IC451
M56788FP
TRK DRIVER
FCS DRIVER
SLD DRIVER
SPDL DRIVER
LOADING DRIVER
IC303
PYY1196
EEPROM
IC701
PE5110B
MODE CONTROL
MICROCOMPUTER
RESET IC
S-806E
FL DISPLAY
PEL1097
KEY MATRIX


INPUT
Lch
Rch
REC VR
34.5744MHz
17.2872MHz
IC802
PCM1800-1
AD CONVERTER
ADLRCK
ADBCK
ADDATA
IC401
DA CONVERTER
IC405
L ch
OUTPUT
R ch
MY, MV TYPES
: PE8001A
KU/CA TYPE
: PCM1718
DALRCK
DADATA
DABCK
IC406
HP
OUTPUT
IC561
BA7082F
VCO IC
IC503
LH64256CK-70
D-RAM
ADDRESS
DATA
16.9344MHz
CDLRCK, CDBCK
CDDATA, CDTX
IC501
LC89585
EFM ENCODER IC
Digital in
COAXIAL
Digital in
OPTICAL
RFOPC(60 pin)
AOUT(61 pin)
DIRBCK
DIRLRCK
DIRDATA
16.9344MHz
AD0-AD7
ADDRESS
IC301
PE5109A
MECH. CONTROL
MICROCOMPUTER
IC502
AD1893JST
Fs CONVERTER
Digital out
COAXIAL
Digital out
OPTICAL
TEMPERATURE
SENSOR IC
TK11041M
MODE
DISPLAY LED
D704
D701
D702

2. PRODUCT DESCRIPTIONS

The PDR-555RW series (PDR-555RW, PDR-V500 and PDR-19RW) is the first series of CD recorders from PIONEER that supports recording and erasing of CD-RW discs. Basic operations with CDs and CD-Rs with this series are based on those of the CD recorders of the PDR-05 series.
The main differences from the PDR-05 series concerning the circuits are:

- The pickup is changed.
- The circuit in RF amplifier is changed.
- The LD drive circuit (including the strategy control circuit) is changed.
- A running OPC circuit is added.
- The focus servo, tracking servo and sled servo are digitized.
- The driver IC is changed.
- The CD decoder IC is changed.
- The sampling rate converter IC is changed.
- The DA converter is changed.

Also, the circuits of the CD recorders of the PDR-509 series are based on those of the PDR-555RW series. So the main circuits used in the PDR-509 series are equivalent to those of the PDR-555RW series. But as an exception, AD converter is changed to the AK5340-VS from the PCM1800-1.

3. PORT TABLE OF MICROCOMPUTER

• The information shown in the list is basic information and may not correspond exactly to that shown in the schematic diagrams.

3.1 MODE CONTROL OF PDR-555RW, PDR-V500 AND PDR-19RW

■ PD4968A (FUNCTION ASSY : IC701)

• Mode Control IC

No.	Mark	Pin Name	I/O	Pin Function
1	FIP6	GRID 6	O	FL grid output 5
2	FIP5	GRID 5	O	FL grid output 6
3	FIP4	GRID 4	O	FL grid output 7
4	FIP3	GRID 3	O	FL grid output 8
5	FIP2	GRID 2	O	FL grid output 9
6	FIP1	GRID 1	O	FL grid output 10
7	FIP0	GRID 0	O	FL grid output 11
8	VDD	–	-	Connect to VDD
9	SCOK	RSCK	O	Serial clock for JIG communication
10	SO0	RSO	O	Serial output for JIG communication
11	SI0	RSI	I	Serial input for JIG communication
12	P24	XTAL	O	XTAL ON/OFF (At digital selection without FS converter : L)
13	P23	XEVCO	O	Encoder VCO ON/OFF (At CD : H)
14	SCK1	FSCK	I/O	Serial clock of the mechanism controller LSI
15	SO1	FSO	O	Serial output of the mechanism controller LSI
16	SI	FSI	I	Serial input of the mechanism controller LSI
17	RESET	XRESET	O	Reset input of the mode controller
18	P74	LDATA	O	Communication data output for LED driver
19	P73	LCLOCK	O	Communication data input for LED driver
20	AVSS	GND	I	Connect to VDD
21	P17	XFUSE	O	During use the serial communication between the mode controller and LC89585 (During use : L)
22	P16	LCK	O	Communication latch output for LED driver
23	P15	XVCO	O	PLL ON/OFF (For SRC ON/OFF SRC OFF: L)
24	P14	FS_THR	O	SRC through output
25	P13	DACLAT	O	Communication latch output for D/A converter
26	P12	XRST	O	Reset output for mechanism controller and ATIP decoder (H: release the reset)
27	P11	XOPT	O	Optical input selection (At optical input selection : L)
28	P10	–	O	Not used (A/D input)
29	AVDD	VDD	–	Connect to VDD
30	AVREF	VDD	–	Connect to VDD
31	P04	ROT_DI	I	For judgement of the rotary encoder SW direction
32	XT2	–	O	Not used
33	VSS	GND	–	Connect to GND
34	X1	–	I	System oscillation 4.19MHz
35	X2	–	O	
36	P37	SW1	I	Demo mode ON/OFF L: Demo display exist
37	P36	MODEL_0	I	Model switching pin
38	P35	MODEL_1	I	
39	P34	MODEL_2	I	
40	P33	RREQ	O	CE output for JIG communication

No.	Mark	Pin Name	I/O	Pin Function
41	P32	MACK	O	Communication response for mechanism controller
42	P31	LREQ	O	CE signal for LC89585
43	P30	UNLOCK	I	Digital unlock detection
44	INTP3	POT_INT	I	Rotary encoder SW operation detection (↓ interrupt)
45	INTP2	XPFAIL	I	Power down detection
46	INTP1	MREQ	I	Mechanism controller communication request (interrupt)
47	INTP0	REMIN	I	Remote control input (interrupt)
48	IC	VPP	I	Connect to GND
49	P72	ISEL3	I	Input selector rotary SW input 3 (H: Analog selection)
50	P71	ISEL2	I	Input selector rotary SW input 2 (H: Optical selection)
51	P70	ISEL1	I	Input selector rotary SW input 1 (H: Coaxial selection)
52	VDD	VDD	–	Connect to VDD
53	P127	SCAN4	O	Key matrix output 4
54	P126	SCAN3	O	Key matrix output 3
55	P125	SCAN2	O	Key matrix output 2
56	P124	SCAN1	O	Key matrix output 1
57	P123	SCAN0	O	Key matrix output 0
58	P122	KEYIN3	I	Key matrix input 3
59	P121	KEYIN2	I	Key matrix input 2
60	P120	KEYIN1	I	Key matrix input 1
61	P117	KEYIN0	I	Key matrix input 0
62	P116	ATT_0V	I	
63	P115	AATLAT	O	
64	P114	FINL_SEG	O	"FINALIZE" segment output (At lights up: H)
65	P113	SEG 10	O	FL segment output 10
66	P112	SEG 9	O	FL segment output 9
67	P111	SEG 8	O	FL segment output 8
68	P110	SEG 7	O	FL segment output 7
69	P107	SEG 6	O	FL segment output 6
70	P106	SEG 5	O	FL segment output 5
71	VLOAD	VLOAD	–	VLOAD
72	P105	SEG 4	O	FL segment output 4
73	P104	SEG 3	O	FL segment output 3
74	P103	SEG 2	O	FL segment output 2
75	P102	SEG 1	O	FL segment output 1
76	P101	SEG 0	O	FL segment output 0
77	P100	GRID10	O	FL grid output 10
78	FIP9	GRID 9	O	FL grid output 9
79	FIP8	GRID 8	O	FL grid output 8
80	FIP7	GRID 7	O	FL grid output 7

3.2 MECHANISM CONTROL OF PDR-555RW, PDR-V500 AND PDR-19RW

■ PD4956B (SERVO DIGITAL ASSY : IC204)

• Mechanism Control IC

No.	Mark	Pin Name	I/O	Pin Function
1	P32/XCLK0/SCL	MSCK	O(I)	Serial transfer clock output of clock synchronous system
2	P33/SO0/SDA	MSO	O(I)	Serial transfer data output of clock synchronous system
3	P34/TO0	–	O	Not used
4	P35/TO1	STCN0	O	Outputs for strategy adjustment (3T delay + 30 nsec)
5	P36/TO2	FOK	I	FOCUS OK input (H: FOCUS OK)
6	P37/TO3	LRST	O	RESET output for the servo and digital system ICs (L: Reset)
7	XRESET	XRESET	I	RESET input (L: Reset)
8	VDD1	+V5	–	Positive power supply excepting port section
9	X2	CLOCK	I	Crystal input for system clock (32MHz)
10	X1	CLOCK	–	Crystal output for system clock (32MHz)
11	VSS1	GND	–	GND excepting port section
12	P00	XECE	O	Enable output for reading the jig for test
13	P01	RECE	O	Laser diode recording power ON/OFF ON: H
14	P02	NC	O	Not used
15	P03	NC	O	Not used
16	P04	IT5SEL	O	Input switch of INTP5 pin (H: SENS, L: TOCP)
17	P05	XENCE	O	External sync enable output of LC89585
18	P06	XASYNC	O	ATIP frame sync
19	P07	XENCE	O(I)	Serial enable output of LC89585
20	P67/XREFRQ/ HLDAK	CLV	O	Spindle servo CLV/CAV mode
21	P66/XWAIT/ HLDRQ	ECLV	O	Spindle servo EFM/Wobble mode
22	P65/XWR	XWR	O	Strobe signal output for READ operation of the external memory
23	P64/XRD	XRD	O	Strobe signal output for WRITE operation of the external memory
24	P63/A19	XLT	O	Latch output of CXD2585Q command
25	P62/A18	SSCK	O	Serial clock output for CXD2585Q command
26	P61/A17	SSO	O	Serial data output for CXD2585Q command
27	P60/A16	ALAT	O	Latch output for AK8563 command
28	P57/A15	SCLK	O	Serial clock output for serial readout of CXD2585Q
29	P56/A14	TP_2P	O	Test pin
30	P55/A13	TP_1P		
31	P54/A12	LDPW4	O	Recording laser power output setting
32	P53/A11	LDPW3		
33	P52/A10	LDPW2		
34	P51/A9	LDPW1		
35	P50/A8	LDPW0		
36	P47/AD7	AD7	O	Data address line
37	P46/AD6	AD6		
38	P45/AD5	AD5		
39	P44/AD4	AD4		
40	P43/AD3	AD3		

No.	Mark	Pin Name	I/O	Pin Function
41	P42/AD2	AD2	O	Data address line
42	P41/AD1	AD1		
43	P40/AD0	AD0		
44	ASTB/CLKOUT	ASTB	O	External latch signal of lower address signal for external memory access
45	Vss0	GND	–	GND of port section
46	TEST	GND	–	Connect to Vss0
47	P10/PWM0	SPSP	O	Spindle drive PWM output in the Spindle CAV
48	P11/PWM1	DGAI	O	In the PLAY or REC mode, it becomes "L" for outer periphery from 18 minutes of the CD and 12cm CD-R, and "H" for outer periphery from 9 minutes of the 8cm CD-R.
49	P12/ASCK2/XSCK2	SQCK	O	Serial clock output for sub-Q of CXD2585Q
50	P13/RXD2/SI2	SQSI	I	Serial data input for sub-Q of CXD2585Q
51	P14/TXD2/SO2	SO2	O	Serial data output
52	P15	MREQ	O	Serial hand shake output to the mode controller
53	P16	D8CM	O	8cm CD-R disc 8cm: H
54	P17	NC	O	Not used
55	VDD0	+5V	–	Positive power supply of port section
56	P70/ANI0	TEPP	I(A)	Tracking error peak to peak (for tracking gain adjustment)
57	P71/ANI1	RFT	I(A)	A/D input of upper side envelope of Playback RF
58	P72/ANI2	RFB	I(A)	A/D input of lower side envelope of Playback RF
59	P73/ANI3	TEMP	I(A)	A/D input of temperature sensor
60	P74/ANI4	RFOPC	I(A)	A/D input of RFOPC/MPXOUT
61	P75/ANI5	VWDC2	I(A)	A/D input for strategy adjustment
62	P76/ANI6	TRAY	I(A)	A/D input of loading position
63	P77/ANI7	AD7	I(A)	Not used
64	AVDD	+5V	–	Positive power supply for A/D converter
65	AVREF1	+5V	–	Reference voltage input for A/D converter
66	AVSS	GND	–	GND for A/D converter
67	ANO0	WREF	O(A)	D/A output for recording APC reference
68	ANO1	VWDC2R	O(A)	D/A output for strategy adjustment
69	AVREF2	+5V	–	Reference voltage for D/A converter
70	AVREF3	GND	–	Reference voltage for D/A converter
71	P20/NMI	XPFAIL	I	Power failure detection AT power failure: falling edge
72	P21/INTP0	FG	I	Spindle FG input
73	P22/INTP1	ATIP	I	ATIP SYNC input
74	P23/INTP2/C1	SCOR	I	Frame sync of CXD2585Q
75	P24/INTP3	SUBSYNC	I	Frame sync of LC89585
76	P25/INTP4/ASCK/ XSCK1	XRFDT	I	EFM playback RF detection
77	P26/INTP5	IT5IN	I	TOC position sensor (TOC position: L), SENS signal input of CXD2585Q
78	P27/SI0	MSI	I	Serial transfer data input of the clock sync. system
79	P30/RXD/SI1	MACK	I	Serial hand shake input to the mode controller
80	P31/TXD/SO1	XFUSE	I	Signal which is during communication between LC89585 and the mode controller

Note: (A) in item I/O shows "ANALOG".

■ PDJ014A (SERVO DIGITAL ASSY: IC205)

External port (External RAM domain (2C000H to 2C0FFH))

No.	Mark	Pin Name	I/O	Pin Function
45	POA0	GAINUP1	O	Gain switch for CD-RW (CD-RW: H)
46	POA1	GAINUP2	O	APC circuit control signal for CD-R running OPC
47	POA2	GAINUP3	O	
48	GND	–	–	GND
49	POA3	ROPC	O	ANI4 input switch (H: RFOPC, L: MPXOUT)
50	POA4	PHYERS	O	Physical Erase
51	POA5	SSEL	O	Tracking envelope detecting reset signal
52	POA6	AGCON	O	AGC circuit ON/OFF for Wobble extraction
53	POA7	LJUNP	O	N track jump
54	POB0	LOUT	O	Loading open
55	POB1	LIN	O	Loading close
56	POB2	KOJK	O	Optical axis switching circuit ON/OFF
57	POB3	EECS	O	Enable output for writing and reading the EEPROM data
58	Vcc	–	–	+5V
59	POB4	STCN4	O	Strategy control output
60	POB5	STCN3	O	
61	POB6	STCN2	O	
62	POB7	STCN1	O	
63	POC0	TEG2	O	Tracking error amplifier gain adjustment
64	POC1	TEG1	O	
65	POC2	TEG0	O	
66	POC3	RW/XR	O	Switch the CD-RW/Other
67	POC4	–	–	Not used
68	GND	–	–	GND
69	POC5	XCD	O	Switch the CD/Other
70	POC6	ENBL	O	LD ON/OFF output
71	POC7	XAMUTE	O	Audio last stage mute

3.3 MODE CONTROL OF PDR-509

■ PE5110B (FUNCTION ASSY : IC701)

• Mode Control IC

No.	Mark	Pin Name	I/O	Pin Function
1	FIP6	GRID 6	O	FL grid output 5
2	FIP5	GRID 5	O	FL grid output 6
3	FIP4	GRID 4	O	FL grid output 7
4	FIP3	GRID 3	O	FL grid output 8
5	FIP2	GRID 2	O	FL grid output 9
6	FIP1	GRID 1	O	FL grid output 10
7	FIP0	GRID 0	O	FL grid output 11
8	VDD	–	–	Connect to VDD
9	SCOK	–	O	Not used "L" outputs
10	SO0	–	O	Not used "L" outputs
11	SI0	–	O	Not used "L" outputs
12	P24	XTAL	O	XTAL ON/OFF (At digital selection without FS converter : L)
13	P23	XEVCO	O	Encoder VCO ON/OFF (At CD : H)
14	SCK1	FSCK	I/O	Serial clock of the mechanism controller LSI
15	SO1	FSO	O	Serial output of the mechanism controller LSI
16	SI	FSI	I	Serial input of the mechanism controller LSI
17	RESET	XRESET	I	Reset input of the mode controller (L : Reset)
18	P74	DISP_L	O	"DISP OFF" LED lights up output (L: lights up)
19	P73	LCLOCK	O	"AUTO/MANUAL" LED lights up output (L: lights up)
20	AVSS	GND	I	Connect to GND
21	P17	XFUSE	O	During use the serial communication between the mode controller and LC89585 (During use : L)
22	P16	CENT_L	O	"CENTER" LED lights up output (L : lights up)
23	P15	XVCO	O	PLL ON/OFF (At digital selection without FS converter : L (PLL oscillation))
24	P14	FS_THR	O	FS through output (Digital input at FS through ON and 44.1kHz : L)
25	P13	DACLAT	O	Communication latch output for D/A converter
26	P12	XRST	O	Reset output for mechanism controller and ATIP decoder (L: reset)
27	P11	XOPT	O	Optical input selection (At optical input selection : L)
28	P10	–	O	Not used "L" outputs (prepare the parallel remote control key inpu)
29	AVDD	VDD	–	Connect to VDD
30	AVREF	VDD	–	Connect to VDD
31	P04	–	–	
32	XT2	–	O	Not used
33	VSS	GND	–	Connect to VDD
34	X1	–	I	System oscillation 4.19MHz
35	X2	–	O	
36	P37	SW1	I	Demo mode ON/OFF (H fixed: No demo mode)
37	P36	FS_SW	I	FS through ON/OFF switching input (H: FS through)
38	P35	HIB_SW	I	Hi-bit mode ON/OFF switching input (H: Hi-bit)
39	P34	LGT_SW	I	LEGATO ON/OFF switching input (H: LEGATO ON)
40	P33	RREQ	O	CE output for jig communication

No.	Mark	Pin Name	I/O	Pin Function
41	P32	MACK	O	Communication response for mechanism controller (H to L: communication permission) (L to H: Communication end)
42	P31	LREQ	O	CE signal for LC89585 (L: Enable)
43	P30	UNLOCK	I	Digital unlock detection
44	INTP3	POT_INT	I	Rotary encoder SW operation detection (↓ interrupt)
45	INTP2	XPFAIL	I	Power down detection (L: power down)
46	INTP1	MREQ	I	Mechanism controller communication request (interrupt)
47	INTP0	REMIN	I	Remote control input (interrupt)
48	IC	VPP	I	Connect to GND
49	P72	ROT3	I	Not used "L" outputs
50	P71	ROT2	I	"H" outputs when playing the CD/CD-R/CD-RW discs in the Hi-bit mode
51	P70	ROT1	I	Rotary encoder SW direction judgment input
52	VDD	VDD	–	Connect to VDD
53	P127	SCAN4	O	Key matrix output 4
54	P126	SCAN3	O	Key matrix output 3
55	P125	SCAN2	O	Key matrix output 2
56	P124	SCAN1	O	Key matrix output 1
57	P123	SCAN0	O	Key matrix output 0
58	P122	KEYIN3	I	Key matrix input 3
59	P121	KEYIN2	I	Key matrix input 2
60	P120	KEYIN1	I	Key matrix input 1
61	P117	KEYIN0	I	Key matrix input 0
62	P116	–	O	Not used "L" outputs
63	P115	SCMS	O	Prepare the mode switch ("L" outputs)
64	P114	FINL_SEG	O	FINALIZE-segment output (At lights up: H)
65	P113	SEG 10	O	FL segment output 10
66	P112	SEG 9	O	FL segment output 9
67	P111	SEG 8	O	FL segment output 8
68	P110	SEG 7	O	FL segment output 7
69	P107	SEG 6	O	FL segment output 6
70	P106	SEG 5	O	FL segment output 5
71	VLOAD	–	–	VLOAD
72	P105	SEG 4	O	FL segment output 4
73	P104	SEG 3	O	FL segment output 3
74	P103	SEG 2	O	FL segment output 2
75	P102	SEG 1	O	FL segment output 1
76	P101	SEG 0	O	FL segment output 0
77	P100	GRID10	O	FL grid output 10
78	FIP9	GRID 9	O	FL grid output 9
79	FIP8	GRID 8	O	FL grid output 8
80	FIP7	GRID 7	O	FL grid output 7

3.4 MECHANISM CONTROL OF PDR-509

■ PE5109A (CD-R CORE ASSY : IC301)

• Mechanism Control IC

No.	Mark	Pin Name	I/O	Pin Function
1	P32/XCLK0/SCL	MSCK	I/O	Serial transfer clock output of clock synchronous system (Set to Input port at not used.)
2	P33/SO0/SDA	MSO	I/O	Serial transfer data output of clock synchronous system (Set to Input port at not used.)
3	P34/TO0	EECS	O	Enable output for writing and reading of the EEPROM data
4	P35/TO1	MREQ	O	Serial hand shake to the mode controller "L"
5	P36/TO2	FOK	I	FOCUS OK input (L: FOCUS OK)
6	P37/TO3	LRST	O	Reset output for the servo and digital system ICs (L: Reset)
7	XRESET	XRESET	I	Reset input (L: Reset)
8	VDD1	+5V	–	+5V
9	X2	CLOCK	–	Crystal input for system clock (32MHz)
10	X1	CLOCK	–	Crystal output for system clock (32MHz)
11	VSS1	GND	–	GND
12	P00	XECE	O	Enable output for reading the jig for test "L"
13	P01	RECE	O	Laser diode recording power ON/OFF ON: H
14	P02	XAMUTE	O	AUDIO last stage mute "L" (according to the mode controller) MUTE ON: during REC/PAUSE, at input selector switch and during STOP
15	P03	TP302	O	"L" outputs
16	P04	TP303	O	"L" outputs
17	P05	XEXSC	O	External sync enable output of LC89585 "L"
18	P06	XASYNC	O	ATIP frame sync "L"
19	P07	XENCE	O(I)	Serial enable output of LC89585 "H" (Set to Input port at not used.)
20	P67/XREFRQ/HLDAK	TP305	O	"L" outputs
21	P66/XWAIT/HLDRQ	TP306	O	"L" outputs
22	P65/XWR	XWR	O	Strobe signal output for read operation of the external memory
23	P64/XRD	XRD	O	Strobe signal output for write operation of the external memory
24	P63/A19	XLT	O	Latch output of CXD2585Q command
25	P62/A18	SSCK	O	Serial clock output for CXD2585Q command
26	P61/A17	SSO	O	Serial data output for CXD2585Q command
27	P60/A16	ALAT	O	Latch output for AK8563 command
28	P57/A15	SCLK	O	Serial clock output for serial readout of CXD2585Q
29	P56/A14	ENBL	O	Laser diode ON/OFF H: ON
30	P55/A13	TP307	O	"L" outputs
31	P54/A12	LDPW4	O	Recording laser power monitor output
32	P53/A11	LDPW3		
33	P52/A10	LDPW2		
34	P51/A9	LDPW1		
35	P50/A8	LDPW0		
36	P47/AD7	AD7	O	Data address line
37	P46/AD6	AD6		
38	P45/AD5	AD5		
39	P44/AD4	AD4		
40	P43/AD3	AD3		

No.	Mark	Pin Name	I/O	Pin Function
41	P42/AD2	AD2	O	Data address line
42	P41/AD1	AD1		
43	P40/AD0	AD0		
44	ASTB/CLKOUT	ASTB	O	External latch signal of lower address signal for external memory access
45	Vss0	GND	–	GND
46	TEST	GND	–	GND
47	P10/PWM0	SPSP	O(A)	Spindle drive PWM output in the Spindle CAV
48	P11/PWM1	LPWM	O(A)	Loading motor output (PWM) AT PWM is not used: "H" (fixed to "H")
49	P12/ASCK2/XSCK2	SQCK	O	Serial clock output for sub-Q of CXD2585Q
50	P13/RXD2/SI2	SQSI	I	Serial data input for sub-Q of CXD2585Q
51	P14/TXD2/SO2	SO2	O	Serial data output
52	P15	TP314	O	"L" outputs
53	P16	TP315	O	"L" outputs
54	P17	TP316	O	"L" outputs
55	VDD0	+5V	–	+5V
56	P70/ANI0	TEPP	I(A)	Tracking error peak to peak (for tracking gain adjustment)
57	P71/ANI1	RFT	I(A)	A/D input of upper side envelope of Playback RF
58	P72/ANI2	RFB	I(A)	A/D input of lower side envelope of Playback RF
59	P73/ANI3	TEMP	I(A)	A/D input of temperature sensor
60	P74/ANI4	RFOPC	I(A)	Running OPC return light 1
61	P75/ANI5	VWDC2	I(A)	Running OPC return light 2
62	P76/ANI6	TRAY	I(A)	A/D input of loading position (OPEN/CLAMP)
63	P77/ANI7	AD7	I(A)	Not used
64	AVDD	Avdd	–	+5V
65	AVREF1	Avref1	–	+5V
66	AVSS	AVss	–	GND
67	ANO0	WREF	O(A)	Recording power 1
68	ANO1	VWDC2R	O(A)	Outputs for strategy setting
69	AVREF2	AVref2	–	+5V
70	AVREF3	AVref3	–	GND
71	P20/NMI	XPFAIL	I	Power failure detection
72	P21/INTP0	FG	I	Spindle FG detection
73	P22/INTP1	ATIP	I	ATIP SYNC detection
74	P23/INTP2/C1	SCOR	I	EFM decoder frame sync detection
75	P24/INTP3	SUBSYNC	I	EFM decoder frame sync detection
76	P25/INTP4/ASCK/-XSCK1	XRFDT	I	EFM playback RF detection
77	P26/INTP5	IT5IN	I	SENS input
78	P27/SI0	MSI	I	Serial transfer DATA input of the clock sync. system
79	P30/RXD/SI1	MACK	I	Serial hand shake CLOCK input to the mode controller
80	P31/TXD/SO1	XFUSE	I	"L" during communicate with the mode controller

Note: (A) in item I/O shows "ANALOG".

■ PDJ014A (CD-R CORE ASSY: IC351)

External port (External RAM domain (2C000H to 2C0FFH))

No.	Mark	Pin Name	I/O	Pin Function
45	POA0	LOUT1	O	Loading open "H"
46	POA1	IN1	O	Loading close "H"
47	POA2	TP366	O	"L" outputs
48	GND	GND	O	GND
49	POA3	TP367	O	"L" outputs
50	POA4	CDROPC	O	Running OPC control output for CD-R
51	POA5	AGCON	O	AGC circuit ON for WOBBLE extraction at CD-R recording section trace
52	POA6	GAINUP1	O	Gain setting for CD-RW
53	POA7	GAINUP2	O	Bias power correction output for CD-RW
54	POB0	ECLV	O	EFM / Wobble CLV mode of the spindle servo
55	POB1	CLV	O	CLV/CAV mode of the spindle servo
56	POB2	DGAI	O	In the PLAY or REC mode, it becomes "L" for outer periphery from 18 minutes of the CD and 12cm CD-R, and "H" for outer periphery from 9 minutes of the 8cm CD-R.
57	POB3	D8CM	O	"H" for 8cm CD-R disc
58	Vcc	VCC	O	+5V
59	POB4	XCD	O	Select SW of the mirror detection circuit CDR/CD (at CD: L)
60	POB5	SSEL	O	Detection reset signal of the tracking error envelope "L"
61	POB6	TP371	O	"L" outputs
62	POB7	TP372	O	"L" outputs
63	POC0	ADD30	O	Strategy assist setting
64	POC1	DOUBLE	O	For double-speed equivalent (at double-speed : H) (Fixed to "L")
65	POC2	RW_XR	O	Switch the CD-RW/Other (at CD-RW: H)
66	POC3	ERAS	O	At Physical erase: "H"
67	POC4	STCN4	O	Strategy control output
68	GND	GND	O	GND
69	POC5	STCN3	O	Strategy control output
70	POC6	STCN2		
71	POC7	STCN1		

4. PIN FUNCTION OF PRINCIPAL IC

• The information shown in the list is basic information and may not correspond exactly to that shown in the schematic diagrams.

4.1 AD1893JST

PDR-555RW, PDR-V500 and PDR-19RW (SERVO DIGITAL ASSY : IC311)
PDR-509 (CD-R CORE ASSY : IC502)

• Sample Rate Converter IC

No.	Pin Name	I/O	Pin Function	No.	Pin Name	I/O	Pin Function
1	N/C	–	Not used	23	N/C	–	Not used
2	BCLK_I	I	Bit clock for input data	24	MODE0_O	I	Serial mode 0 control for output port
3	WCLK_I	I	Word clock for input data	25	BKPOL_O	I	Bit clock polarity L: Normal mode
4	LR_I	I	L/R clock for input data	26	N/C	–	Not used
5	N/C	–	Not used	27	GND	–	Ground
6	VDD	–	Power supply	28	VDD	–	Power supply
7	GND	–	Ground	29	N/C	–	Not used
8	N/C	–	Not used	30	DATA_O	O	Serial output, MSB fast
9	BKPOL_I	I	Bit clock polarity L: Normal mode	31	LR_O	O	L/R clock for output data
10	MODE0_I	I	Serial mode 0 control for input port	32	WCLK_O	O	Word clock for output data
11	N/C	–	Not used	33	N/C	–	Not used
12	N/C	–	Not used	34	N/C	–	Not used
13	MODE1_I	I	Serial mode 1 control for input port	35	BCLK_O	O	Bit clock for output data
14	XRESET	I	Reset signal L: Reset	36	PWRDWN	I	Power down input H: Low consumption electric power state
15	N/C	–	Not used	37	N/C	–	Not used
16	GND	–	Ground	38	SETSLW	I	Settling against the change in the sampling rate H: Slow, L: Fast
17	N/C	–	Not used	39	N/C	–	Not used
18	MUTE_I	I	Mute input	40	XTAL_O	O	Crystal output
19	N/C	–	Not used	41	N/C	–	Not used
20	MUTE_O	O	Mute output	42	XTAL_I	I	Crystal input
21	MODE1_O	I	Serial mode 1 control for output port	43	DATA_I	I	Serial input, MSB fast
22	N/C	–	Not used	44	N/C	–	Not used

4.2 PYY1196

PDR-555RW, PDR-V500 and PDR-19RW (FUNCTION ASSY : IC705)
PDR-509 (CD-R CORE ASSY : IC303)

• EEPROM

No.	Pin Name	I/O	Pin Function
1	NC	–	Non connection
2	VCC	–	Power supply
3	CS	I	Chip select input
4	SK	I	Serial clock input
5	DI	I	Start bit, operation code, address and serial data input
6	DO	O	Serial data output and indication output of READY/XBUSY internal state
7	GND	–	Ground
8	NC	–	Non connection

4.3 LC89585

PDR-555RW, PDR-V500 and PDR-19RW (SERVO DIGITAL ASSY : IC308)
PDR-509 (CD-R CORE ASSY : IC501)

• EFM Encoder IC

No.	Pin Name	I/O	Pin Connection
1	DIN1	I	Digital input 1
2	DIN2	I	Digital input 2
3	DIN3	I	Digital input 3
4	DIN4	I	Digital input 4
5	DIRRC1	I	RC oscillation input of DIR section
6	DIRRC2	O	RC oscillation output of DIR section
7	AVDD	–	Analog power supply
8	DIRRS	I	VCO oscillation band-pass adjustment input of DIR section
9	AGND	–	Analog ground
10	DIRVCO	I	VCO oscillation setting input of DIR section
11	DIRLPF	O	Low-pass filter of DIR section
12	VSS	–	Ground
13	VDD	–	Power supply
14	DIRCK	O	DIR system clock output
15	DIRBCK	O	DIR bit clock output
16	DIRLRCK	O	DIR LR clock output
17	DIRDATA	O	DIR demodulation data output
18	DIRWDCK	O	DIR word clock output
19	DIRU	O	User bit output
20	DIRERR	O	Data error or monitor output of lock state H: Unlock, L: Lock
21	DRAMSW	I	External DRAM capacity setting input H: 14MHz, L: 1MHz
22	CJSDATA	I	Data input of the clock jitter absorption circuit section
23	CJSBCK	I	Bit clock input of the clock jitter absorption circuit section
24	CJSLRCK	I	LR clock input of the clock jitter absorption circuit section
25	JITVCOIN	I	VCO input of the clock jitter absorption circuit section
26	JITLPFO	O	LPF output of the clock jitter absorption circuit section
27	JITLPFI	I	LPF input of the clock jitter absorption circuit section
28	JITPCO	O	Phase comparison output of the clock jitter absorption circuit section
29	JITERR	O	Lock state monitor output of the clock jitter absorption circuit section H: Unlock
30	DACDATA	O	DAC data output
31	DACBCK	O	DAC bit clock output
32	DACLRCK	O	DAC LR clock output
33	ADCDATA	I	ADC data input
34	ADCCLK	O	ADC clock output
35	ADCBCK	O	ADC bit clock output
36	ADCLRCK	O	ADC LR clock output
37	ADCSTBY	O	ADC standby signal output H: Operate, L: Standby
38	XTALIN	I	System clock input
39	XTALOUT	O	System clock output
40	VSS	–	Ground
41	VDD	–	Power supply
42	DACCKOUT	O	DAC system clock output
43	ENCCKOUT	O	System clock output of CD decoder
44	CDDAT	I	Data input of CD decoder
45	CDBCK	I	Bit clock input of CD decoder
46	CDLRCK	I	LR clock input of CD decoder
47	CDTX	I	Digital out signal input of CD decoder
48	DITOUT	O	Digital out signal output
49	TP6	I	Test pin
50	XRESET	I	Reset pin L: Reset

No.	Pin Name	I/O	Pin Connection
51	TP7	I	Test pin
52	XCAS	O	DRAM row-address strobe signal
53	XOE	O	DRAM output enable signal
54	A8	O	DRAM address
55	A7	O	
56	A6	O	
57	A5	O	
58	A4	O	
59	A3	O	
60	A2	O	
61	VDD	–	Power supply
62	VSS	–	Ground
63	A1	O	DRAM address
64	A0	O	
65	A9	O	
66	XRAS	O	DRAM column address strobe signal
67	XWR	O	DRAM writing/reading signal
68	DQ2	I/O	DRAM data input/output
69	DQ1	I/O	
70	DQ4	I/O	
71	DQ3	I/O	
72	TP0	I	Test pin
73	TP1	I	
74	TP2	I	
75	TP3	I	
76	ENCVCOIN	I	Clock input of the encode circuit
77	ENCLPFO	O	LPF output of the encode circuit
78	ENCLPFI	I	LPF input of the encode circuit
79	ENCPCO	O	Phase comparison output of the encode circuit
80	ENCERR	O	Lock state monitor output of the encode circuit H: Unlock
81	TP4	O	Test pin
82	TP5	I	
83	XRFDET	I	RF detection signal input L: RF exist, H: no RF
84	RECEN	I	Recording enable signal input L: Recording impossible, H: Recording possible
85	XSAMPLE	O	Sample hold pulse output
86	DET4T	O	4T detecting signal output
87	DET3T	O	3T detecting signal output
88	EFM	O	EFM signal output
89	VDD	–	Power supply
90	VSS	–	Ground
91	ENCCK	O	Encoder clock input
92	XEXTACK	O	ATIP synchronous signal output
93	XEXTSYNC	I	ATIP synchronous enable signal input
94	ATIPSYNC	I	ATIP synchronous signal
95	SUBSYNC	O	Subcode synchronous signal output
96	CCB	I	Select signal of the CPU interface L: General purpose serial, H: Sanyo CCB format
97	CE	I	Chip enable input of the CPU interface
98	CL	I	Data transfer clock input of the CPU interface
99	DI	I	Data input of the CPU interface
100	DO	O	Data output of the CPU interface

4.4 LH64256CK-70

PDR-555RW, PDR-V500 and PDR-19RW (SERVO DIGITAL ASSY : IC301)
PDR-509 (CD-R CORE ASSY : IC503)

• DRAM

No.	Pin Name	I/O	Pin Function	No.	Pin Name	I/O	Pin Function
1	I/O3	I/O	Data 3	14	A4	I	Address 4
2	I/O4	I/O	Data 4	15	A5	I	Address 5
3	XWE	I	Write enable	16	A6	I	Address 6
4	XRAS	I	Row address strobe	17	A7	I	Address 7
5	NC	–	Not used	18	A8	I	Address 8
–	–	–	–	–	–	–	–
9	A0	I	Address 0	22	XOE	I	Output enable
10	A1	I	Address 1	23	XCAS	I	Column address strobe
11	A2	I	Address 2	24	I/O1	I/O	Data 1
12	A3	I	Address 3	25	I/O2	I/O	Data 2
13	VCC	–	Power supply	26	VSS	–	Ground

4.5 PA9004A or PA9007A

PDR-555RW, PDR-V500 and PDR-19RW (SERVO DIGITAL ASSY : IC247)
PDR-509 (CD-R CORE ASSY : IC201)

• CDR Servo Amp.

No.	Pin Name	I/O	Pin Function	No.	Pin Name	I/O	Pin Function
1	VDD	–	Power supply	33	VCC1	–	Power supply
2	PWM1	I	CAV PWM input	34	TEG3	I	
3	PWM2	I	Wobble CLV PWM input	35	CTR	I	
4	PWM2O	O	Wobble CLV PWM output	36	TEDET	O	
5	PWM2+	I	Connect a capacitor for Wobble CLV LPF	37	BIAS	I	
6	PWM3	I	EFM CLV input	38	WBL1-	I	
7	PWM3+	O	EFM CLV output	39	WBL1O	O	
8	SPDL-	I		40	WBL2-	I	
9	SPDLO	O		41	WBL2O	O	
10	REFV	O		42	WBL3-	I	
11	GND1	–	Ground	43	WBL3O	O	
12	REFIN	I		44	WBLC-	I	
13	CLV	I	Spindle switching signal	45	WBLCO	O	
14	ECLV	I	Spindle switching signal	46	GND2	–	Ground
15	SPDL	O		47	RFB	O	
16	FWREV	O		48	RFB+	I	
17	FGOUT	O	FG output	49	RFT	O	
18	VEE1	–		50	RFT+	I	
19	FGIN	I	FG input	51	RFOPC	I	RF OPC signal input
20	Q0	I	DA converter setting pin for LD power	52	HF	I	HF signal input
21	Q1			53	VEE2	–	
22	Q2			54	CBL	I	
23	Q3			55	CPL	I	
24	Q4			56	CDRMR1	O	CDR mirror
25	LDPWO	O		57	CDRMR2	I	
26	TEG0	I	Tracking servo gain setting pin	58	CDRMRC	I	
27	TEG1			59	RFDT-	I	
28	TEG2			60	RFREF	I	
29	TE	I	Tracking error input	61	RFDET	O	RF detecting signal output
30	TEO	O	Tracking error signal output after the gain set	62	XCD	I	
31	TRKG-	I		63	MIRR	O	Mirror signal output
32	TRKER	O		64	VCC2	–	

4.6 PDJ014A

PDR-555RW, PDR-V500 and PDR-19RW (SERVO DIGITAL ASSY : IC205)
PDR-509 (CD-R CORE ASSY : IC351)

• ATIP Decoder

No.	Pin Name	I/O	Pin Function	No.	Pin Name	I/O	Pin Function
1	WBL	I	Wobble input	41	XCE0	O	Chip enable output 0
2	FSK	O	FSK demodulation signal output	42	XCE1	O	Chip enable output 1
3	SBSY	I	Subcode sync. input Normally: 75Hz	43	XCE2	O	Chip enable output 2
4	MDP	O	MDP output for CLV servo	44	XCE3	O	Chip enable output 3
5	SPSEL	I	CPU interface select H: Serial, L: Parallel	45	POA0	I/O	General purpose input/output Gain switch for CD-RW (CD-RW: H)
6	ASYNC	O	ATIP sync. output	46	POA1	I/O	General purpose input/output AC circuit control signal for CD-R running OPC
7	ACK	I	Serial interface clock input	47	POA2	I/O	General purpose input/output
8	GND	–	Ground	48	GND	–	Ground
9	AOUTPE	I	Serial data read enable	49	POA3	I/O	General purpose input/output ANI4 input switch (H: RFOPC, L: MPXOUT)
10	AOUT	O	Serial data output 32 bits	50	POA4	I/O	General purpose input/output Physical Erase
11	AINPE	I	Serial data write enable input	51	POA5	I/O	General purpose input/output Reset signal of tracking error envelope detection
12	AIN	I	Serial data input 16 bits	52	POA6	I/O	General purpose input/output AGC circuit ON/OFF for Wobble extraction
13	XCK	I	Master clock input Normal speed: 4.3218MHz	53	POA7	I/O	General purpose input/output N track jump
14	XSRST	I	System reset L: reset	54	POB0	O	General purpose output Loading open
15	SIOK	O	Special information standby flag output H: Readout possible	55	POB1	O	General purpose output Loading close
16	CRCOK	O	CRC calculation result output H: CRC OK, L: CRC NG	56	POB2	O	General purpose output Optical axis switching circuit ON/OFF
17	PROTECT	O	ATIP sync. protection state output H: Protection, L: Non-protection	57	POB3	O	General purpose output Enable output for writing and reading the EEPROM data
18	VCC	–	Power supply	58	VCC	–	Power supply
19	NC	–	Not used	59	POB4	O	General purpose output Strategy control output
20	XADSEL	I	Start address setting strobe input of address decoder	60	POB5	O	
21	XWE	I	Write enable input of the microcomputer	61	POB6	O	
22	XRE	I	Read enable input of the microcomputer	62	POB7	O	
23	SYA0	I	Address bus of the microcomputer	63	POC0	O	General purpose output Tracking error amp gain adjustment
24	SYA1	I		64	POC1	O	
25	SYA2	I		65	POC2	O	
26	SYA3	I		66	POC3	O	General purpose output Switch the CD-RW/other
27	SYA12	I		67	POC4	O	General purpose output Not used
28	GND	–	Ground	68	GND	–	Ground
29	SYA13	I	Address bus of the microcomputer	69	POC5	O	General purpose output Switch the CD/other
30	SYA14	I		70	POC6	O	General purpose output LD ON/OFF output
31	SYA15	I		71	POC7	O	General purpose output Audio last stage mute
32	SYD0	I/O	Data bus of the microcomputer	72	TESTB	I	Test pin
33	SYD1	I/O		73	TEST	I	Test pin
34	SYD2	I/O		74	TEST0	I	Test pin
35	SYD3	I/O		75	TEST1	I	Test pin
36	SYD4	I/O		76	TEST2	I	Test pin
37	SYD5	I/O		77	TEST3	I	Test pin
38	VCC	–	Power supply	78	VCC	–	Power supply
39	SYD6	I/O	Data bus of the microcomputer	79	TEST4	I	Test pin
40	SYD7	I/O		80	PREL_PSTH	I	

4.7 PDK033A [PDR-555RW, PDR-V500 and PDR-19RW (SERVO DIGITAL ASSY : IC316)] PDK041A [PDR-509 (CD-R CORE ASSY : IC431)]

• Strategy Control IC

No.	Pin Name	I/O	Pin Function	No.	Pin Name	I/O	Pin Function
1	NC	–	Not used	25	ODON	O	Over-drive control H: over-drive ON
2	XRESET	I	Reset L: Reset	26	NC	–	Not used
3	NC	–	Not used	27	W_XR	O	Writing/reading signal output H:writing
4	CK34M	I	Clock input	28	NC	–	Not used
5	NC	–	Not used	29	WLDON	O	Write LD control
6	CK17M	O	2 dividing output of CK17M	30	VDD	–	Power supply
7	NC	–	Not used	31	GND	–	Ground
8	WFPDSH	O	Sample pulse output for Write APC	32	RWLDON	O	CD-RW LD ON/OFF
9	NC	–	Not used	33	NC	–	Not used
10	SAMPLE	O	Sample hold pulse output	34	REWLDON	O	Switch the CD, CD-R/CD-RW
11	NC	–	Not used	35	NC	–	Not used
12	OPCSH	O	Sample hold pulse output for OPC	36	NC	–	Not used
13	NC	–	Not used	37	STCN1	I	Starategy select 1
14	NC	–	Not used	38	STCN2	I	Starategy select 2
15	CK4M	I	4.3218MHz input	39	STCN3	I	Starategy select 3
16	NC	–	Not used	40	STCN4	I	Starategy select 4
17	EFMIN	I	EFM input	41	NC	–	Not used
18	NC	–	Not used	42	ERASE	I	ERASE control
19	XSAMPLE	I	Sample hold pulse input	43	NC	–	Not used
20	NC	–	Not used	44	RW_XR	I	Switch the CD-R/CD-RW
21	RECE	I	Recording enable signal input	45	NC	–	Not used
22	NC	–	Not used	46	DOUBLE	I	Switch the normal speed/double speed
23	TST1	I	Test pin Connect to ground	47	NC	–	Not used
24	NC	–	Not used	48	ADD30	I	Outputs for strategy adjustment (3T delay + 30)

4.8 AK5340-VS

PDR-555RW, PDR-V500 and PDR-19RW only (AUDIO ASSY : IC801)

• A/D Converter IC

No.	Pin Name	I/O	Pin Function
1	AINL+	I	L ch analog non-inverting input
2	AINL-	I	L ch analog positive-phase input
3	VREFIN	I	Reference voltage input
4	VA+	–	Analog power supply
5	AGND	–	Analog ground
6	NC	–	Not used
7	NC	–	Not used
8	TST1	–	Test pin
9	SEL18	I	Output data length select L: 16 bits, H: 18 bits
10	PD	I	Power down H: Power down
11	TST2	–	Test pin
12	CMODE	I	Master clock select L: 256 fs, H: 384 fs
13	SMODE	I	Interface clock select L: Slave mode, H: Master mode
14	L/XR	I	LR clock input
15	SCLK	I	Serial data clock input
16	SDATA	O	Serial data output
17	FSYNC	I	Output enable of SDATA H: Enable
18	VDP+	–	Digital power supply
19	DGND	–	Digital ground
20	CLK	I	Master clock input
21	TST3	–	Test pin
22	TST4	–	Test pin
23	NC	–	Not used
24	VDB+	–	Digital power supply
25	NC	–	Not used
26	VREF	O	Reference voltage output (VA+) – 2.6V
27	AINR-	I	R ch analog non-inverting input
28	AINR+	I	R ch analog positive-phase input

4.9 PD0236AD

PDR-19RW only (AUDIO ASSY : IC451)

• Hi-Bit IC

No.	Pin Name	I/O	Pin Function
1	BCSEL	I	fs select of the bit clock
2	DASEL	I	Output length select in the bit expansion function ON
3	LRSEL	I	Polarity select of LRCKO
4	LRCKO	O	LR clock output
5	BCKO	O	Bit clock output
6	DATAO	O	Data output
7	GND	–	Ground
8	NC	–	Non connection
9	NC	–	Non connection
10	VDD	–	Power supply
11	LRCKI	I	LR clock input
12	DATAI	I	Data input
13	BCKI	I	Bit clock input
14	NC	–	Non connection
15	SEL	I	Bit length expansion process/Input data output select
16	XRST	I	Reset pin H: Normal, H: Reset

4.10 PCM1800-1

PDR-509 only (AUDIO ASSY : IC802)

• A/D Converter

No.	Pin Name	I/O	Pin Function
1	VINL	I	Analog input L ch
2	VREF1	–	Decoupling capacitor of reference 1
3	REFCOM	–	Reference decoupling common
4	VREF2	–	Decoupling capacitor of reference 2
5	VINR	I	Analog input R ch
6	RSTB	I	Reset input Active "L"
7	BYPAS	I	LCF bypass control
8	FMT0	I	Audio data format 0
9	FMT1	I	Audio data format 1
10	MODE0	I	Master/Slave mode selection 0
11	MODE1	I	Master/Slave mode selection 1
12	FSYNC	I/O	Frame sync input/output
13	LRCK	I/O	Sampling clock input/output
14	BCK	I/O	Bit clock input/output
15	DOUT	O	Audio data output
16	SYSCLK	I	System clock input 256fs, 384fs or 512fs
17	DGND	–	Digital GND
18	VDD	–	Digital power supply
19	CINNR	–	Anti-aliasing filter capacitor (–), R ch
20	CINPR	–	Anti-aliasing filter capacitor (+), R ch
21	CINNL	–	Anti-aliasing filter capacitor (–), L ch
22	CINPL	–	Anti-aliasing filter capacitor (+), L ch
23	VCC	–	Analog power supply
24	AGND	–	Analog GND

5. RECORDING MECHANISM FOR CD-Rs AND CD-RWs

5.1 DISC

The PDR-555RW is capable of recording on CD-R discs and of recording and overwriting on CD-RW discs.
A CD-R has a triple-layered structure (from the bottom, the pigment recording layer, reflective layer, and protective layer) on a polycarbonate substrate, as shown in Fig. 5-1.
There are three kinds of pigments: cyanic pigments, phthalocyanin pigments, and azo pigments. And there are two kinds of reflective layer: gold and silver.
To record on the disc, a laser beam is shot at the pigment recording layer to form pits by transforming the pigments by heat.
When the disc is played, the difference in reflectivity between areas with converted pigments and unconverted pigments is read as a signal.

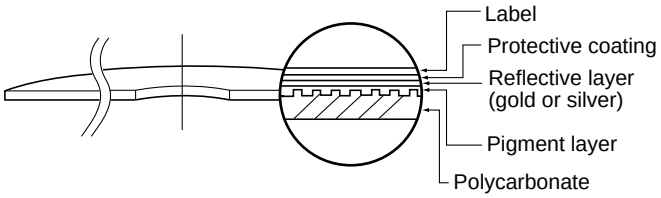


Fig. 5-1 CD-R disc

The more complex CD-RW has a five-layered structure (from the bottom, a dielectric layer, phase-change recording layer, another dielectric layer, reflective layer, and protective layer) on a polycarbonate board, as shown in Fig. 5-2.
The phase-change recording layer is a colloid of chalcogen substances. such as AG-In-Sb-Te4 and Ge-Sb-Te. It becomes a liquid layer when heated to a high temperature (about 500°C to 700°C), with its atomic structure chaotic. And after being cooled rapidly, it becomes solid, with its atomic structure still chaotic> It is non-crystal (in an amorphous state).
It reaches a crystalline state after being heated to a lower temperature (about 200°C) and being cooled gradually. Lands and pits are made on the disc by repeating this procedure.
The reflectance is small when the layer is noncrystalline (in an amorphous state), and it is large when the layer is crystalline. This difference in reflectivity is read as a signal when the disc is played.

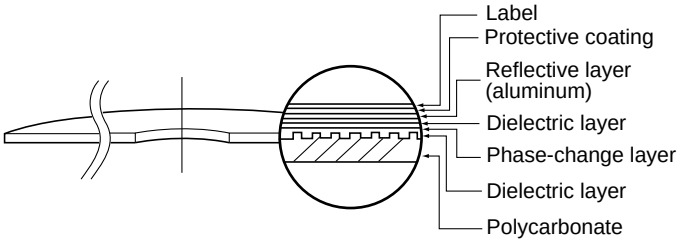


Fig. 5-2 CD-RW disc

Transformation of CD-RW

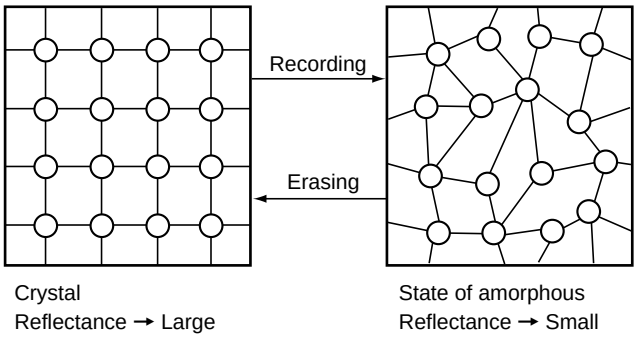


Fig. 5-3 Transformation of CD-RW

5.2 OVERWRITE RECORDING OF CD-RW

CD-RWs adopt overwriting. New recording can be made in an area with previous recording as shown in Fig. 5-4.

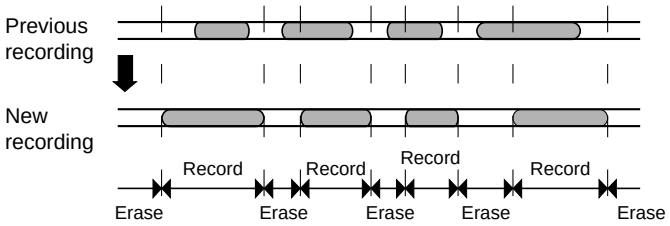


Fig. 5-4 Overwrite recording of CD-RW

6. PICKUP (KRS-200A)

The pickup of the PDR-555RW employs the 3-beam differential push-pull method.

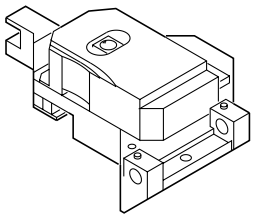
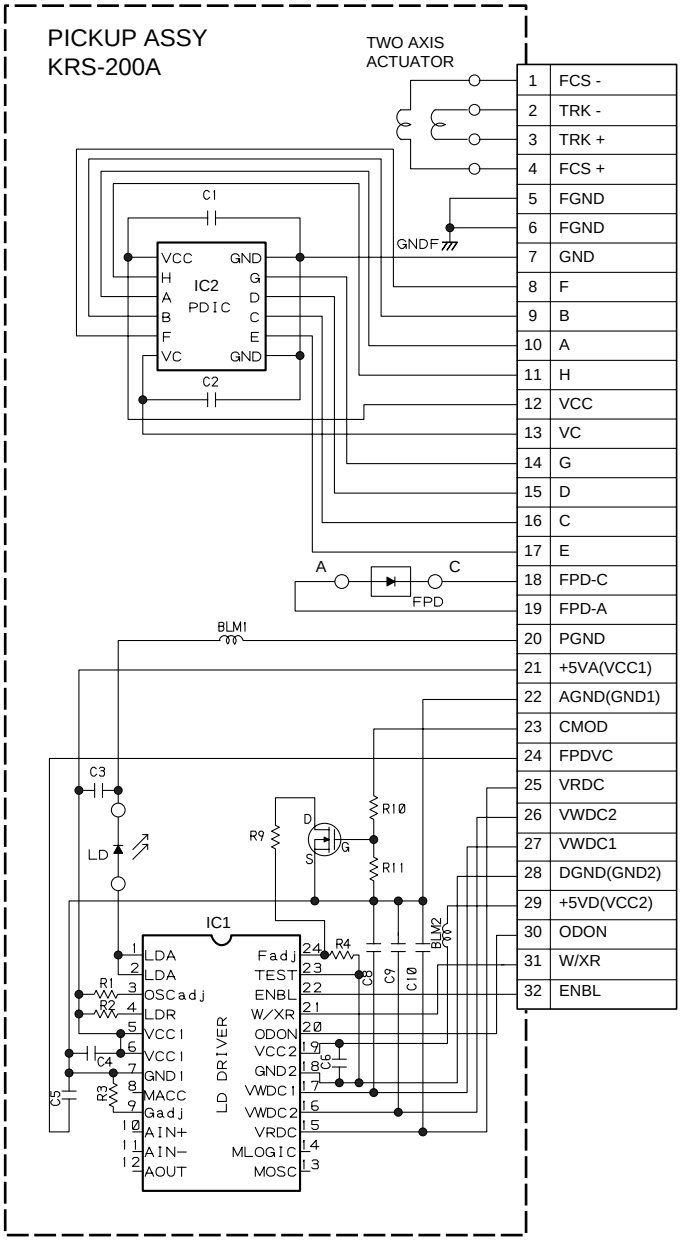


Fig. 6-1 KRS-200A

The pickup is incorporated with a drive IC for the laser diode. The surrounding circuits are designed as shown in Fig. 6-2 :



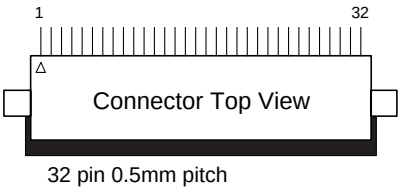


Fig. 6-2 Surrounding circuit of the pickup

7. CIRCUIT DESCRIPTIONS

7.1 SERVO CIRCUITS

7.1.1 Control Circuit for the Laser Diode

This circuit controls the optical output of the laser diode. It has two systems of APC circuit that keep the optical output of the laser diode constant.
One is the APC circuit for playing power of CD/CD-R/CD-RW and for erasing power while recording on CD-RW, and the other is for the recording power while recording on a CD-R or CD-RW.
Each adjustment VR is used for the adjustments shown below.

VR101 (VR101) PB.PW : Playing power adjustment
VR102 (VR163) R REC.PW1 : CD-R recording power adjustment
VR103 (VR162) R REC.PW2 : CD-R overdrive adjustment
VR104 (VR141) RW REC.PW0 : CD-RW bias power adjustment
VR106 (VR164) RW REC.PW1 : CD-RW erasing power adjustment
VR105 (VR161) RW REC.PW2 : CD-RW recording power adjustment
( )In the inside, for PDR-509.

The semi-fixed VRs shown above adjusts the points shown in Fig. 7-1 and 7-2.

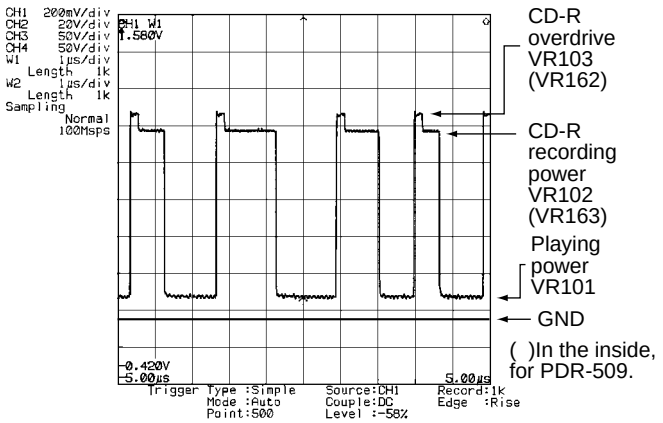


Fig. 7-1 CD-R recording waveform

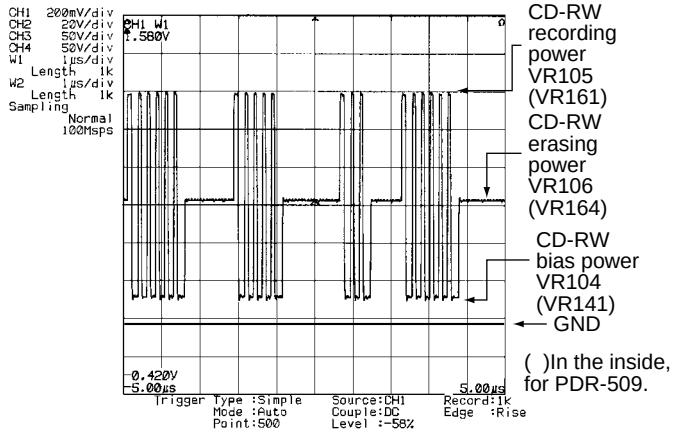


Fig. 7-2 CD-RW recording waveform

7.1.2 Error Signal Generation Circuit

Employing the 3-beam differential push-pull method, the pickup has a photodetector that divides the main beam in four and two detectors that divide the subbeam in two. HF, RF, Wobble, focus error, and tracking error signals are generated from the voltage signal output.

7.1.3 Focus Servo

The focus servo employs the same astigmatism method as that of conventional CD players.
The focus signal generated in the RF processor IC (AK8563, IC103-pin 11) is input to the decoder IC (CXD2585Q, IC353-pin 39).
The signal processed in the IC is output from pins 29 and 30. This output signal is input to the driver IC (BA5932FP, IC352), and is used to drive the focus actuator of the pickup.

7.1.4 Tracking Thread Servo

The tracking servo is also the same as that of conventional CD players.
The tracking error signal generated in the RF processor IC (AK8563, IC103-pin 10) is input to the decoder IC (CXD2585Q, IC353-pin 41) and CDR servo amplifier IC (PA9004A, IC247-pin 29).
The signal processed in the decoder IC is output from the pins 31 and 32. This output signal is input to the driver IC (BA5932FP, IC352), and is used to drive the tracking actuator of the pickup.
The signal input to the CDR servo amplifier IC is input to the mechanism control (IC204-pin 56) as the P-P value for tracking and used for detecting the tracking error level.
The tracking error signal also functions as the control signal of the sled.

7.1.5 Spindle Servo

The spindle servo has four modes: Stop, CAV, EFM-CLV and Wobble-CLV.
The EFM-CLV used for playing a CD is also used for playing a recorded CD-R or CD-RW. The A, B, C, and D signals that correspond to the four divisions of the main beam output from the pickup are generated in IC102 and IC101 as RF signals.
These RF signals are input to the decoder IC (CXD2585Q, IC353-pin 43). MDP (pin 25) of a triple-value PWM signal from the sync signal extracted from RF signal and internal standard signal.
When unrecorded parts of a CD-R or CD-RW are played, the rotation control signal called Wobble is read out from the guide groove of the disc. This Wobble signal is output from the RF processor IC (AK8563, IC103-pin 46), runs through the bandpass filter of the CDR servo amplifier IC (PA9004A, IC247), and becomes the Wobble-CLV signal in the ATIP decoder IC (PDJ014A, IC205).
In addition to the Wobble servo, the ATIP decoder IC decodes information, such as ATIP sync, absolute time, recommended recording power, lead-in area start time, lead-out start time and disc application code, from the Wobble signal, and sends the information to the mechanism-control microcomputer.
If a sudden change in the rotation of the spindle motor is required, such as upon start, stop, and search, FG is read to detect the rotation of the spindle motor in the servo mechanism assembly for CAV

control. The spindle motor is controlled by switching the above three spindle servos (CAV, EFM-CLV and Wobble-CLV) and Stop mode by controlling the switch of the servo amplifier IC (PA9004A, IC247) according to the control signal output from the mechanism-control microcomputer.

7.2 DEFECT CIRCUIT

The defect signal is output if there is a defect, such as a flaw, on the disc. If the defect signal is "Hi," the tracking error is muted and the low-frequency component of the error signal output just before the defect occurs is applied to the focus error and the spindle error so that the pliability rises.

7.3 EFM-DIGITAL PLL

Channel clocks are required to demodulate the EFM signal reproduced from the optical system, because it is modulated to 3T to 11T (where T is a cycle of the channel clock), which is integer multiple of T. Practically, the PLL must read the channel clock because the irregularities in the spindle rotation may change the pulse width of the EFM signal.
This product has three stages of PLL. The first stage is a wide-range PLL. The output of the first-stage PLL functions as the standard for all clocks in CXD2585Q.
The PLL of the second stage is for generating high-frequency clock indispensable for the digital PLL of the third stage.
The PLL of the third stage is a digital PLL for generating the practical channel clock.

7.4 RF DETECTION

For CD-Rs there is an RF detection circuit to distinguish recorded and unrecorded parts. The detection signal is output from the servo amplifier IC (PA9004A, IC247-pin 61).
RFB and RFT also output the peak value and the bottom value of the HF signal used for OPC operation.

7.5 MIRROR CIRCUIT

A mirror signal equivalent to that of conventional CD players is used for CDs with EFM signals and for recorded parts of CD-Rs and CD-RWs.
For unrecorded parts of a CD-R or CD-RW, the mirror signal peculiar to the CD decoder is generated using the RC (radial contrast) generated by crossing a groove.

7.6 AUDIO CIRCUITS

7.6.1 Analog Audio Input

The audio signal input via JA801 runs through the volume of the VR Assy once and returns to the AUDIO Assy.
The input buffer circuit of IC803 (L-channel) and IC804 (R-channel) is a single-ended/differential conversion circuit composed inverting-inverting circuits.
The audio signal is converted to a differential signal and input to the IC801 A/D converter (AK5340-VS).

7.6.2 A/D Converter

AK5340-VS, made by Asahi Chemical is used as the A/D converter. This is an 18-bit, 2-channel A/D converter, which employs fifth-generation delta-sigma techniques.
It contains two delta-sigma modulators and performs s 64-times oversampling of both channels simultaneously.
The input range of the A/D converter is 4.0 Vp-p. So it becomes 0 dB when a signal of 2.08 Vp-p is input to input terminals AIN+ and AIN-.
The control signals of the A/D converter are ADSTBY (pin 10), ADLRCK (pin 14), ADBCLK (pin 15), and ADDATA (pin 16).
ADSTBY (pin 10) switches to Power-Down mode at "Hi" and offset calibration begins upon falling from "Hi" to "Lo."
During the offset calibration, the input of each channel is measured as the data for it. At this moment, each audio input terminal is separated from the outside and short-circuited inside.
ADLRCK (pin 14) is the signal from the encoder IC (IC308 LC89585, pin 36), and ADBCLK (pin 15) and ADDATA (pin 16) are signals for the encoder IC (pins 35 and 33).

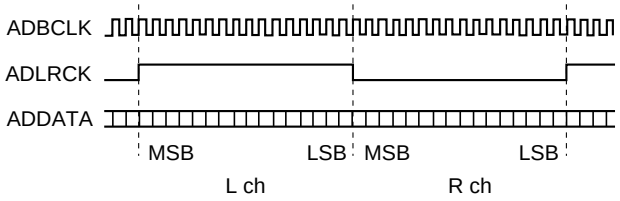


Fig. 7-3 AK5340-VS data output timing

However, A/D Converter of PDR-509 uses PCM1800-1 made by the BURR-BROWN company.

7.6.3 Hi-bit IC (PDR-19RW Only)

The PDR-19RW has a Hi-bit IC. It transforms 16-bit audio data from the encoder into 24-bit audio data.

7.6.4 D/A Converter

The PE8001A is used as the D/A converter (the PDR-509/KU/CA uses the PCM1716).
The PE8001A can switch the characteristics of digital filters. The switching is made in accordance with the serial data output from the mode-control microcomputer. The digital filter settings are switched depending on the product destination, as shown in the table below:

Types of the Digital Filter	Models/Destinations
Normal digital filter	PDR-555RW/KU/CA PDR-V500/KU/CA PDR-509/KU/CA(using PCM1716)
Legato link	PDR-555RW/MY PDR-19RW/KU/CA PDR-509/MY

(With the PCM1716, switched between normal digital filter and slow roll off)
"Enhanced multilevel sigma-delta techniques" are employed for the DAC block. They convert the output from the digital filter block into an 8-level sigma-delta modulation signal. Their anti-jitter efficiency of the operation clock is superior to that of the normal 1-bit DAC.

7.6.5 Analog Audio Output Block

The output from the D/A converter is output via the buffer amplifier, which has a gain of about 7 dB.
There are two audio-mute circuits. One is a mute circuit controlled by a microcomputer, and the other is a zero-detection circuit controlled by the ZERO terminal of the D/A converter.
This ZERO terminal outputs a signal when the audio input to the D/A converter becomes Infinity or Zero for both channels.

7.7 DIGITAL CIRCUITS

7.7.1 Digital Audio Interface Input Block

There are two systems of digital interface input: coaxial and optical. The coaxial input is sent to IC308 (LC89585, pin 4) via the duty-ratio adjustment circuit composed of IC313 (TC74HC00AF) and IC314 (NJM2940M), after its waveform being adjusted by IC305 (TC74HCU04AF).
The optical digital input (JA301 (GP1F32R) output) is sent to IC308 (LC89585, pin 1) via the duty-ratio adjustment circuit, composed of IC313 (TC74HC00AF) and IC314 (NJM2940M).
The PDR-509 has no waveform adjustment circuit in the digital input block.

7.7.2 Sampling Rate Converter

The AD1893JST, the asynchronous type, is used as the sampling rate converter.
The sampling rate converter is bypassed as for PDR-509 when the sampling rate of the input is 44.1kHz.

7.7.3 Clock-jitter Suppressor Circuit (PDR-509 only)

The clock-jitter suppresser circuit of the encoder IC is used to absorb the jitter from the digital interface receiver when the sampling rate converter is in through mode.

7.7.4 Data Selector

The DIR block output, the clock-jitter suppressor block output, or the 384-fs clock input from the XTALIN terminal is output from the DACCKOUT and ENCCKOUT terminals in accordance with a signal from the microcomputer.

7.7.5 Digital Fader, Level Meter, Mute Blocks

The output range of the digital fader block is +17.99 to -66.22 dB.
The level meter interface block provides the data select output and the fader output. The selected input data are processed to provide total 16-bit data for L channel and R channel. The level meter interface block has a zero detection circuit, which outputs to microcomputer interface block when detecting that the input data to both channels are all zero.
Muting can be turned on/off for the output from the fader block. The digital volumes of the PDR-509 also use this block. The variable range is +12 dB to -48 dB.

7.7.6 Memory Control

The encoder IC can control an external D-RAM (1 or 4 Megabits). It receives signals from the mute block, the clock-jitter suppressor block and the encode block.

7.7.7 EFM Encoding

Subcode P and Q and the digital audio data from the D-RAM control block are EFM-modulated.
At the same time, subcodes, sync and a merge bit are added. Then, it is NRZI-converted and encoded to EFM signals of the CD format.

7.7.8 Strategy Control

Whereas the signal of 3T to 11T (T=231 nsec) is obtained in the EFM encoder block, the LD power-on time is adjusted in recording so that the pit length becomes ideal for playback.
Specifically, pulses 3T to 11T are processed for -1T and output as 2T to 10T.
However, the optimum pulse width in recording slightly differs depending on the disc types. The PDK033A (strategy control IC) of IC316 performs fine adjustment of this pulse width.
For PDR-509, Strategy control IC becomes IC431 PDK041A.

7.7.9 Digital Audio Interface Modulation

The digital audio interface modulation block receives signals from the CD decoder (IC353, CXD2585Q), DIR block (through input), and A/D converter (IC801, AK5340-VS).
The input signals are converted to the digital audio interface and output from DITOUT (pin 48). The signals are output in the CP1201 (EIAJ) civilian format.

8. DETAILED DESCRIPTIONS OF OUTPUT TERMINAL CONTROL

The terminals controlled by the microcomputer are set in each mode as follows:

8.1 DGAI (microcomputer,pin 48) and D8CM (microcomputer, pin 53) For PDR-509 : DGAI (ATIP decoder,pin 56) and D8CM (ATIP decoder, pin 57) TERMINAL CONTROL

	DGAI	D8CM
TEST mode	L	L
Normal mode		
Not for spindle CLV	L	L
For spindle CLV		
Playing the outer periphery from 18 minutes in absolute time	H	–
Recording on the outer periphery from 18 minutes in absolute time	H	–
CD-R/RW whose program area is less than thirty minutes (regarded as an 8-cm disc)	–	H
Others	L	L

8.2 AGCON (ATIP decoder, pin 52) For PDR-509 : AGCON (ATIP decoder, pin 51) TERMINAL CONTROL

	AGCON
Recording	L
Not recording with RF	H
Not recording without RF	L

8.3 XCD (ATIP decoder, pin 69)
For PDR-509 :
XCD (ATIP decoder, pin 59)
TERMINAL CONTROL

	XCD
After inserting a disc	
CD	L
CD-R (New disc)	H
CD-R (Partial disc)	H
CD-R (Finalized disc)	L
CD-RW (New disc)	H
CD-RW (Partial disc)	H
CD-RW (Finalized disc)	H
After finalizing	
CD-R (Partial disc)	H → L
CD-RW (Partial disc)	H → H
Finalized disc After All Track Erase	H → H
Finalized disc After TOC Erase	H → H

8.4 GAINUP1 (ATIP decoder, pin 45)
RW/XR (ATIP decoder, pin 66)
For PDR-509 :
GAINUP1 (ATIP decoder, pin 52)
RW/XR (ATIP decoder, pin 65)
TERMINAL CONTROL

	GAINUP1, RW/XR
After inserting a disc	
CD	L
CD-R (New disc)	L
CD-R (Partial disc)	L
CD-R (Finalized disc)	L
CD-RW (New disc)	H
CD-RW (Partial disc)	H
CD-RW (Finalized disc)	H
Recording CD-RW (GAINUP1 is set to "L" in the circuit.)	H
Judging the FZC disc	L
In CD-RW REC setting average	L

8.5 CDROPC (ATIP decoder, pin 46)
For PDR-509 :
CDROPC (ATIP decoder, pin 50)
TERMINAL CONTROL

	CDROPC
Performing CD-R running OPC AC circuit control ON	H (400 msec after starting recording)
During PCA count or TEST REC	L
During PMA REC	L

8.6 GAINUP3 (ATIP decoder, pin 47)
For PDR-509 :
RWBIAS (ATIP decoder, pin 53)
TERMINAL CONTROL

	GAINUP3
Temperature rises over 45°C	H → L
Temperature falls under 40°C	L → H
The upper end of limitation	NG when exceeded
The lower end of limitation	NG when exceeded

8.7 PHYERS (ATIP decoder, pin 52)
For PDR-509 :
ERAS (ATIP decoder, pin 66)
TERMINAL CONTROL

	PHYERS
During All Disc Erase	H
During PCA Erase	H

8.8 SSEL (ATIP decoder, pin 51)
For PDR-509 :
SSEL (ATIP decoder, pin 60)
TERMINAL CONTROL

	SSEL
Adjusting the TEG error level	H

8.9 ENBL (ATIP decoder, pin 70)
For PDR-509 :
ENBL (Microcomputer, pin 29)
TERMINAL CONTROL

	ENBL
When LD is ON	H

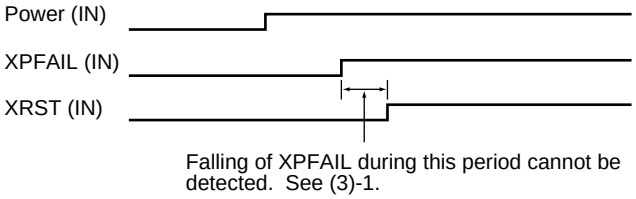
9. OPERATION DESCRIPTIONS

9.1 ABOUT POWER ON/OFF

9.1.1 Power-up (When the power outlet is active)

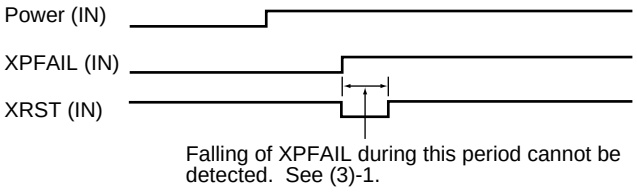
9.1.1.1 Without Backup Power Supply. (When the content of RAM of the microcomputer is cleared.)

(1) The power turns on.
(2) XPFAIL becomes "H".
(3) The reset of the microcomputer then becomes "H" and the microcomputer starts operating. Immediately after the microcomputer starts operating, it confirm that XPFAIL = "H."
(3)-1 If XPFAI L= "L," the microcomputer immediately returns to STOP mode (power-save mode). In this case, backup process is not performed.



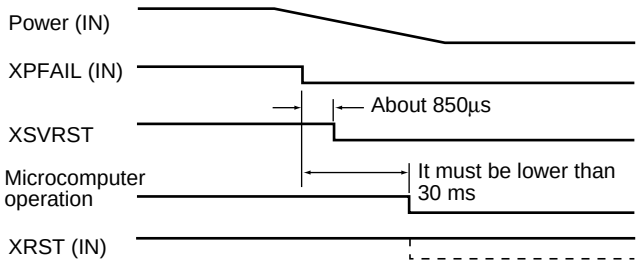
9.1.1.2 With Backup Power Supply

(1) The power turns on.
(2) XPFAIL becomes "H," and the reset of the microcomputer becomes "L" at the same time.
(3) The reset of the microcomputer then becomes "H," and the microcomputer exits STOP mode and starts operating. Immediately after the microcomputer starts operating, it confirm that XPFAIL = "H."
(3)-1 If XPFAI L= "L," the microcomputer immediately returns to STOP mode (power-save mode) again. In this case, backup process is not performed.



9.1.2 Power Down (When the power outlet is not active or power failure occurs)

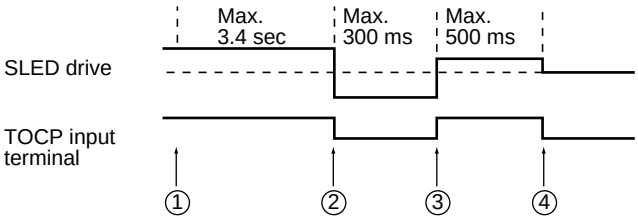
(1) The power starts turning off, and XPFAIL becomes "L" when the power voltage decreases to some extent.
(2) Interrupted at XPFAI L= "L," and the current operating mode, disc data, etc. are backed up.
(3) As the reset may become "L" about 3 ms after XPFAIL become L," the microcomputer must enter STOP mode (power-save mode) before that. (This is because resumption is made without data backup if the microcomputer is reset before it enters STOP mode.)
In STOP mode, the reset is pulled up by the backup power supply.



9.2 ABOUT SERVO CONTROL

9.2.1 Seek Track 0

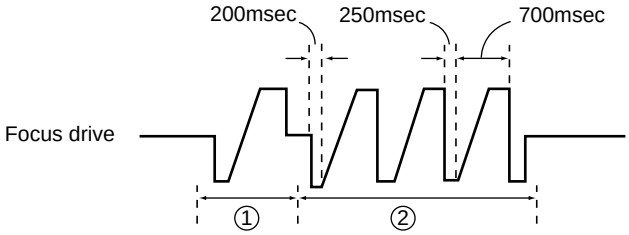
The sled is carried to the TOC area (home position).



① When TOCP is "H," the sled starts moving toward the inner periphery.
② When TOCP becomes "L," the sled moves toward the outer periphery.
③ When TOCP becomes "H," the sled slowly moves toward the inner periphery.
④ When TOCP becomes "L" (detected by an interruption), the sled stops, and the operation finishes.

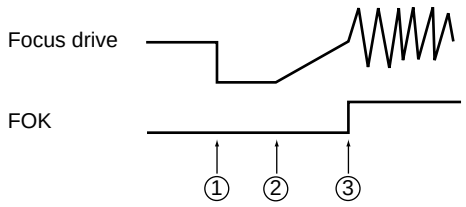
9.2.2 Focus ON

9.2.2.1 Without a Disc



① Temporally judging FZC
② Executing focus IN

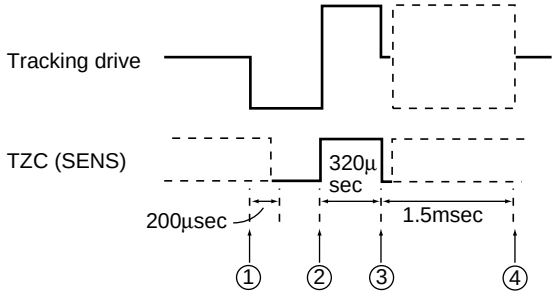
9.2.2.2 With a Disc



① Focus down (preparing for auto focus)
② Starting auto focus
③ Focus IN

9.2.3 One-Track Jump (Direct Sequence)

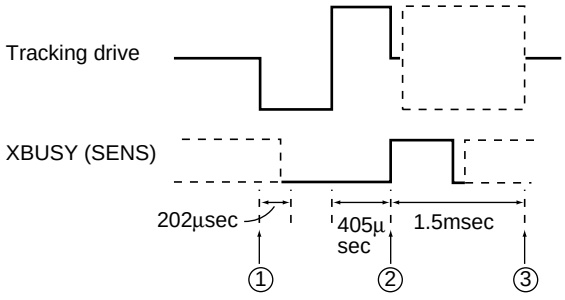
Used for CD-R/RW only.



① Starts KICK. TZC blind time: 200 µs
② Detects TZC rising in FWD (or falling in REV).
Starts BREAK. BREAK time: 320 µs.
③ Detects TZC falling in FWD (or rising in REV).
④ Finishes GAIN-UP after 1.5 ms.

9.2.4 One-Track Jump (Auto Sequence)

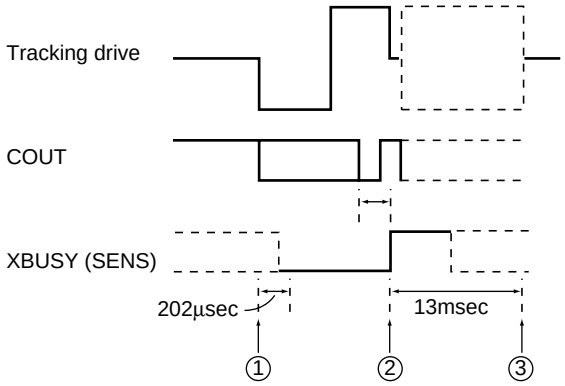
Used for CD/Finalized CD-R only.



① Starts the auto sequence (starts a jump).
② Detects XBUSY (SENS) rising. (The auto sequence ends.)
③ Finishes GAIN-UP after 1.5 ms.

9.2.5 Ten-Track Jump

Used for CD/CD-R/CD-RW.

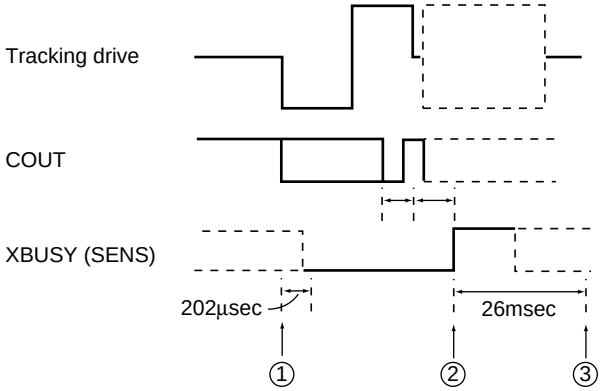


① Starts the auto sequence (starts a jump).
② Detects XBUSY (SENS) rising. (The auto sequence ends.)
③ Finishes GAIN-UP after 13 ms (1 loop).

∗ : The auto sequence ends when the cycle of COUT exceeds Overflow C (405 µs).

9.2.6 2N-Track Jump

Used for CD/Finalized CD-R only.

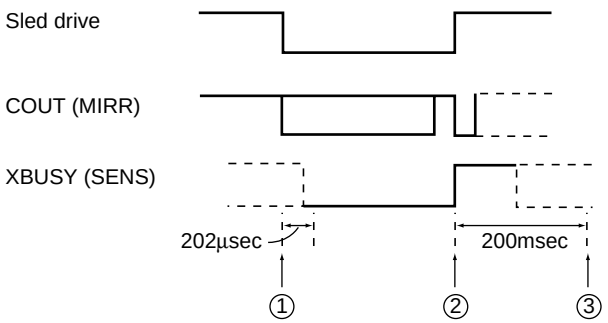


① Starts the auto sequence (starts a jump).
② Detects XBUSY (SENS) rising. (The auto sequence ends.)
③ Finishes GAIN-UP after 26 ms (2 loops).

∗ : The auto sequence ends after KICK (D) when the cycle of COUT exceeds Overflow C (405 µs).

9.2.7 M-Track Move

Used for CD/Finalized CD-R only.

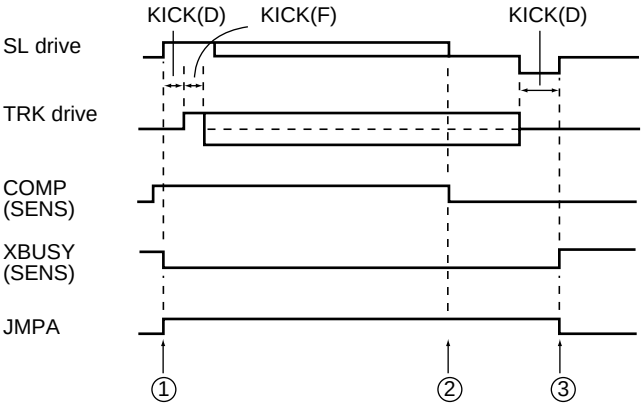


① Starts the auto sequence (starts a jump).
② Detects XBUSY (SENS) rising. (The auto sequence ends.)
③ Executes tracking ON processing after 200 ms

9.2.8 Fine Search

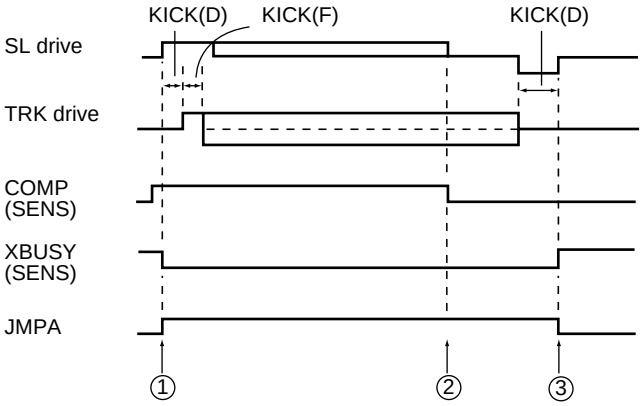
Used for CD-R/RW. There are two formats of Fine Search: M-Track Move format and 2N-Track Jump format, which are used depending on the conditions.

9.2.8.1 M-Track Move Format



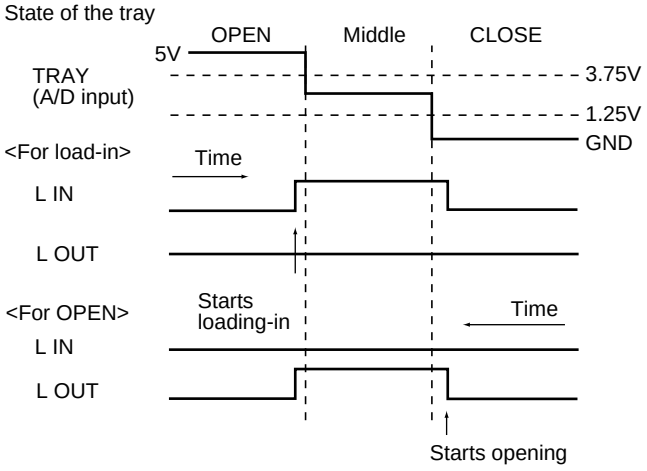
① Starts Fine Search (starts a jump).
② Detects COMP falling.
③ Detects XBUSY (SENS) rising. (The auto sequence ends.)

9.2.8.2 2N-Track Jump Format



① Starts Fine Search (starts a jump).
② Detects COMP falling.
③ Detects XBUSY (SENS) rising. (The auto sequence ends.)

9.2.9 Loading Control



9.2.9.1 Load-in Operation

Starts the load-in operation by setting LIN to "H."
Regards that CLOSE is finished if the TRAY(A/D) input becomes lower than 1.25 V, and finishes the operation by setting LIN to "L."

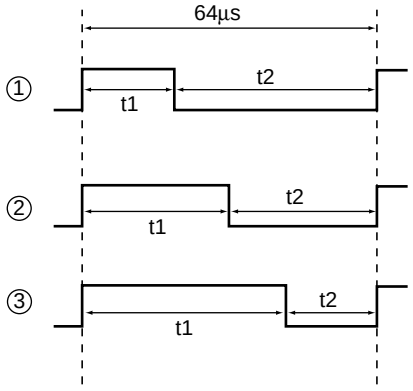
9.2.9.2 Open Operation

Starts the open operation by setting LOUT to H."
Regards that OPEN is finished if the TRAY(A/D) input becomes higher than 3.75 V, and finishes the operation by setting LOUT to L."

9.2.10 Spindle Control

9.2.10.1 Spindle Control

The spindle is controlled using the PWM output from the SPSP terminal.
The microcomputer controls it only for CAV control.



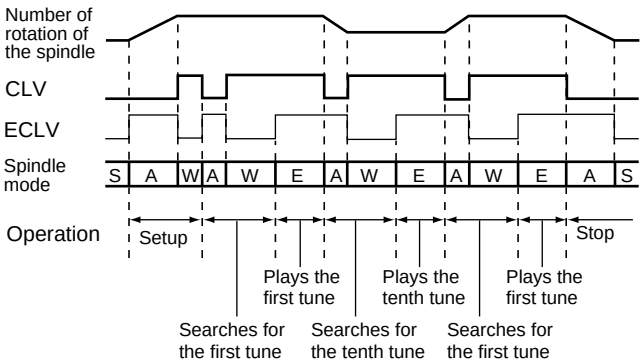
① Kicking
The current velocity is slower than the target velocity.
(The velocity decreases upon spindle start-up, searching the inner periphery or in CAV.)

② Neutral
The target velocity and the current velocity are the same.
(In STOP, or during CAV lock)

③ Breaking
The current velocity is faster than the target velocity.
(The velocity increases upon spindle breaking, searching the outer periphery or in CAV.)

9.2.10.2 Spindle Servo Mode Switching

Spindle mode switching in CD-R STOP → PLAY → Search → STOP operations is shown below:



Spindle mode: S = STOP (in stop state)
A = CAV
W = Wobble CLV
E = EFM CLV

9.3 ERASING (CD-RW ONLY)

9.3.1 Last-Track-Erase Operation

The Last-Track-Erase function is to erase the last track of a partial CD-RW disc.

∗ Writing to PMA is performed when the tray is opened or at the next opportunity of PMA writing.

9.3.2 All-Track-Erase Operation

9.3.2.1 All-Track-Erase of a Partial CD-RW Disc

This function is to erase all tracks of a partial CD-RW disc.

∗ Writing to PMA is performed when the tray is opened or finished with the next PMA writing.

9.3.2.2 All-Track-Erase of a Finalized CD-RW Disc

This function is to return a finalized CD-RW disc to the state of a blank CD-RW disc so that recording can be made on it again.

9.3.3 TOC-Erase Operation

TOC-Erase is the function to restore a finalized CD-RW disc to a partial CD-RW disc so that additional recording can be made on it again.

9.3.4 All-Disc-Erase Operation

All-Disc-Erase is the function to restore the recorded CD-RW disc (with pits on it) to the state of a blank CD-RW disc (with no pits).

9.3.5 PCA-Erase Operation

PCA-Erase is the function to automatically erase PCA when the PCA-area runs out in PCA recording.

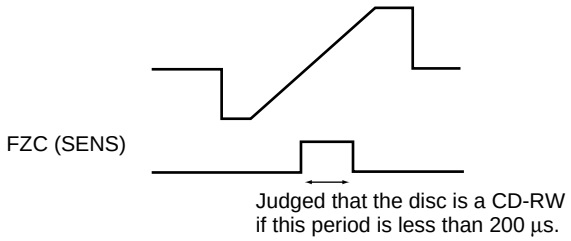
9.4 RID CODES

With an audio CD recorder code, the Recorder Identification (RID) codes are recorded in subcode Q channel mode 3 of a disc.
The content written in RID code is the maker code, type code (product model number), and identification code (serial number).

9.5 DISC JUDGMENT

9.5.1 Tentative Judgment Using FZC (Distinguishing Between CD/CD-R and CD-RW)

The judgment is made before the Focus IN operation after the disc is inserted.



Bringing up the focus, the range of FZC is checked at that time.
It is judged that the disc is a CD/CD-R if FZC remains "H" for more than 200 µs.
It is judged that the disc is a CD-RW if FZC is not detected or intermittently detected.

9.5.2 Disc Judgment with Each Type of Disc

<CD-RW>

1 : Blank Disc

① Disc that has no RF in LIA and PMA
- Brand-new disc
- Disc after ALL Disc Erase processing

② Disc that has RF in PMA, but not in LIA
- Disc that has only MODE2 in PMA
  Disc of category ① , calibrated once and ejected.
- Disc that has MODE0 in PMA
  Disc of category ① , with ALL Track Erase processing executed after recording, and ejected

③ Disc of MODE0 data while it has RF in LIA and PMA
- Disc processed with only an ALL Track Erase operation after being finalized

2: Partial Disc (Disc which has RF in PMA)

④ Disc that does not have RF in LIA

⑤ Disc that has RF in LIA
- Disc processed with ALL Track Erase operation and recorded on after being finalized

3: Finalized Disc (Disc that has TOC in LIA)

⑥ Disc that does not have RF in PMA
- Disc finalized with synchronized recording

⑦ Disc that has RF in PMA

<CD-R> Orange book Ver. 2.9/3.0

1: Blank Disc

⑧ Disc that does not have RF in LIA and PMA
- Brand-new disc

⑨ Disc that has RF in PMA, but not in LIA
- Disc that has only MODE2 in PMA
  Disc of category ⑧ , calibrated once and ejected.

2: Partial Disc (disc that has RF in PMA)

⑩ Disc that does not have RF in LIA

3: Finalize Disc (Disc that has TOC in LIA)

⑪ Disc that does not have RF in PMA
- Disc finalized with synchronized recording

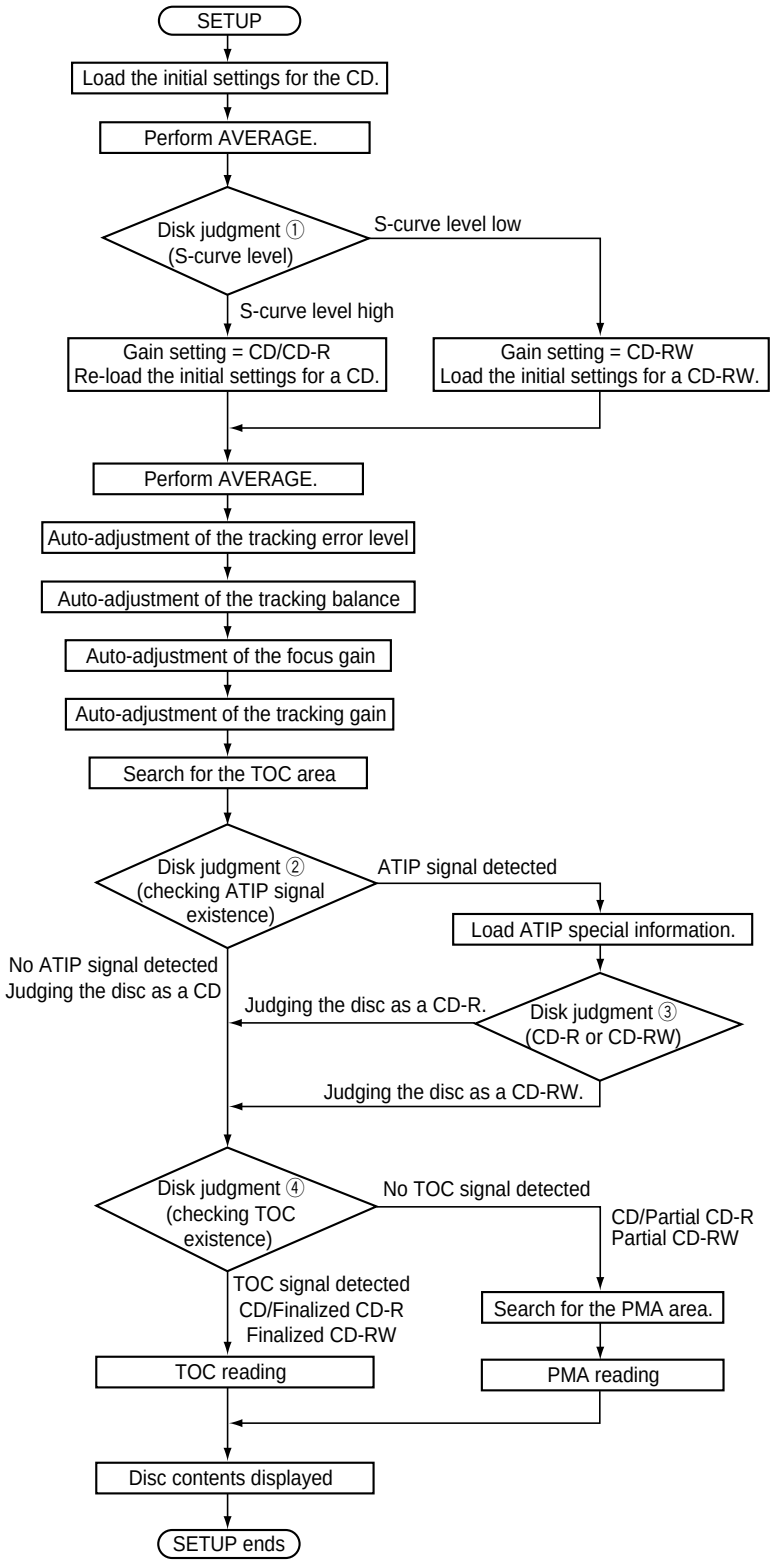
⑫ Disc that has RF in PMA

<CD>

⑬ 12cm CD
⑭ 8cm CD
⑮ CD-ROM
⑯ CD Extra
⑰ CD-I
⑱ CDV
⑲ Maxi-CD
⑳ Others

Note) LIA : Lead In Area
PMA : Program Memory Area

9.6 SETUP (FLOW)



Servo Condition

FOC Servo	TRK Servo	SPINDL Servo
OFF	OFF	STOP
OFF	OFF	STOP
OFF	OFF	STOP
OFF	OFF	STOP
OFF	OFF	STOP
ON	OFF	CAV
ON	OFF	CAV
ON	ON	CAV
ON	ON	CAV
ON	ON	W-CLV or RF-CLV
ON	ON	W-CLV
ON	ON	RF-CLV
ON	ON	W-CLV
OFF	OFF	STOP

9.6.1 Verification of Disc Judgments

1. Tentative judgment by FZC (distinguishing between CD/CD-R and CD-RW)

2. Tentative judgment by checking the RF existence at TOCP

< If RF exists >

The disc may be a finalized CD or CD-R/RW or an erased CD-RW.
If the disc was judged to be a CD-RW in FZC tentative judgment, it remains judged as a CD-RW (the disc status is CD-R).
If the disc was judged to be a CD/CD-R in FZC tentative judgment, it is tentatively judged to be a CD.

< If RF does not exist >

The disc has strong likelihood of CD-R or CD-RW.
If the disc was judged as CD-RW in FZC tentative judgment, it is judged as CD-RW. If the disc was judged to be a CD/CD-R in FZC tentative judgment, it is judged to be a CD.

3. Tentative judgment (3) by checking the RF existence in LIA (99:00:00)

When the setup is finished with the results of tentative judgments 1 and 2, the RF existence is verified while searching for LIA (99:00:00) and executing AGC (gain adjustment).

< If RF exists >

The results of the tentative judgment indicates:
The CD may be a CD.
The CD-R may be a finalized CD-R.
The CD-RW may be finalized CD-RW or erased CD-RW.

< If RF does not exist >

The result of the tentative judgment indicates:
CD → no possibility
The CD-R may be a partial CD-R or blank CD-R.
The CD-RW may be a partial CD-RW or blank CD-RW.

4. Disc determination by reading the ATIP special information

If the result of tentative judgment indicates the disc is a CD-RW, and ATIP also indicates it is a CD-RW, the disc is determined to be a CD-RW.
In the tentative judgment by checking the RF existence in LIA (99:00:00):

If RF exists	→	Loads TOC, as there is a possibility that the disc is a finalized CD-RW.
If no RF exists	→	Makes a decision depending on the result of PMA loading, since the disc may be a partial CD-RW or blank CD-RW.

If both the result the tentative judgment and ATIP do not indicate it is a CD-RW, the disc is determined to be a CD-R.

In the tentative judgment by checking the RF existence in LIA (99:00:00):

If RF exists	→	Loads TOC, as there is a possibility that the disc is a finalized CD-R.
If no RF exists	→	Makes a decision depending on the result of PMA loading, since the disc may be a partial CD-RW or blank CD-R.

When the ATIP special information cannot be read, the disc is determined to be a CD.

If the results of FZC tentative judgment and ATIP indicate it to be of a different type, a retry is made by reversing the result of FZC tentative judgment.

5. Disc-type determination by reading TOC

If MODE0 data are detected while reading TOC with CD-RW, the disc status is changed to Partial CD-RW and the operation shifts to PMA reading.

9.6.2 Auto-Adjustments

9.6.2.1 Calibration of Tracking Offset Adjust Ability and Verification of the Temperature Sensor

These are carried out upon POWER ON and SETUP.

(1) Calibration of the tracking offset adjustment ability

- When ADR_RFB and ADR_RFT are 1.5 to 3 V, the values are stored in VRB_REF and VRT_REF respectively.
- When ADR_RFB are ADR_RFT are not 1.5 to 3 V, the mode-control computer is notified through the TOKNG_F setting that the initial values for the RF envelope signal cannot be obtained. In this case, the mode-control computer generates a STOP command if the setup step is before PCA. The values are stored in VRB_REF and VRT_REF, respectively.

(2) Verification of the temperature sensor

Upon POWER ON, the temperature sensor is checked whether the sensor shows a value within -15°C to 70°C. If it is out of the range, the sensor is judged defective, and subsequent operations are made in the temperature sensor defect status.

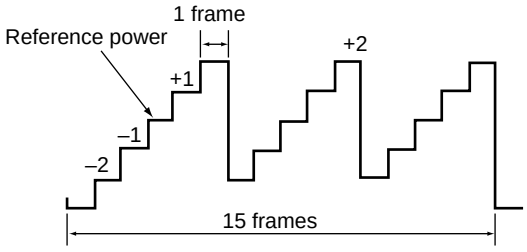
9.6.3 Tracking Error Level Adjustment and Disc Determination

The tracking error level adjustment and disc determination are simultaneously executed when a disc is inserted. The tentative judgment made in this stage checks the RF existence in the lead-in area. If RF exists, the disc is tentatively judged to be a CD. If no RF exists, the disc is tentatively judged to be a CD-R.
However, if the result of the tentative judgment using FZC indicates it is a CD-RW, the disc is determined as CD-R regardless of the RF existence.

9.6.4 Recording Power Sweep Mode for Recording Power Calibration

9.6.4.1 Sweep recording on CD-R

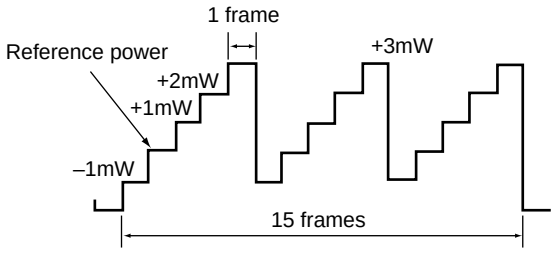
- Sweep recording of ±2 steps of the reference power is made three times.



Recording Power Sweep

9.6.4.2 Sweep recording on a CD-RW

- Sweep recording of -1 mW to +3 mW of the reference power is made three times.



Recording Power Sweep

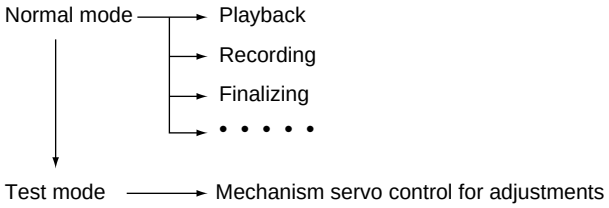
9.6.5 Playback RF Estimating Mode for Recording Power Calibration

The PCA TEST area recorded in Recording Power Sweep mode is played back to check the RF waveform and find the optimum recording power.

10. ABOUT TEST MODE OPERATIONS

Test mode is provided to permit you to easily achieve adjustments and confirmation required for servicing.
When you set the unit to Test mode, the front-panel keys have different functions from these in Normal mode. By operating these keys in the specified sequence, you can perform the required adjustments and confirmations.

Relationship between Test mode and Normal mode



[Setting the unit to Test mode]

You can set the unit to Test mode with the following procedure:

1. Turn off the power.
2. Short-circuit the pattern for Test mode.
3. Turn on the power.
   (When the unit enters Test mode, RAM information of the mechanism control is cleared.)

If Test mode is set correctly, displays different from those in ordinary power-up state are obtained. (All the FL indicators light, and REC LED lights in amber. (For PDR-509, REC LED lights in red.))
If the displays are the same as those in the normal mode, Test mode may not have been set correctly. Repeat steps 1 to 3 above.

Caution: Before setting the unit to Test mode, be sure to set the INPUT selector to ANALOG.
If the selector is not set to ANALOG, malfunctions may occur in Adjustment mode.

[Releasing Test mode]

You can release Test mode with the following procedure:
1. Press the STOP key to stop all operations.
2. Turn off the power.

[Key Functions in Test Mode]

Operations common to Adjustment modes and other modes

Key Name	Operation in Test Mode	Descriptions
FINALIZE	Focus servo close	Turns on the laser diode with the playback power, slowly moving up the focus actuator after moving it down, and closes the focus servo where the focus of the object lens is obtained. If you gently rotate the disc in stop state in this condition by fingers, you may hear the sound generated when the focus servo is operating correctly. If you press the key without loading a disc, the laser diode lights. The focus actuator repeats up and down movements three times after the first down movement, then it returns to the original position.
PLAY	Spindle Servo ON	Starts up the spindle motor for clockwise rotation, and sets the spindle servo to closed loop when the rotation speed of the disc reaches the specified value (about 500 rpm at the inner periphery).
PAUSE	Tracking Servo close/open	If you press this key in a condition that the focus servo and the spindle servo is correctly in a closed loop, the tracking servo is set to a closed loop, the current track number and the elapsed time are displayed on the front panel, and the playback signal is output. If the elapsed time is not displayed, if it does not count up regularly, or if the audio is not counted correctly, there may be a defect in the outer peripheral no-sound area of the disc, poor maintenance or other problems. The key functions as a toggle switch. Each press of the key opens or closes the tracking servo in turn. If you press this key without loading a disc, no change occurs.
Key common to MANUAL SEARCH REV and TRAK/MANUAL REV	Carriage Reverse (toward the inner periphery)	Transports the pickup toward the inner periphery of a disc. If you press the key when the tracking servo is in a closed loop, the loop automatically opens. In Test mode, sufficient care must be taken when operating this key, since the motor does not automatically stop even when the pickup reaches the physical end.
Key common to MANUAL SEARCH FWD or TRACK/MANUAL FWD	Carriage Forward (toward the outer periphery)	Transports the pickup to the outer periphery of a disc. If you press the key when the tracking servo is in a closed loop, the loop automatically opens. In Test mode, sufficient care must be taken when operating this key, since the motor does not automatically stop even when the pickup reaches the physical end.
STOP	Stop	Stops all servos and returns them to their initial states. However, the pickup stays in the position it was in when the STOP key was pressed.
OPEN/CLOSE	Disc tray open/close	Opens and closes the disc tray. This key functions as a toggle switch. Each push open or close the disc tray in turn. When you press the key while the disc is rotating, the disc tray opens after the rotation of the disc stops.
REC ↓ REC MUTE	Playback power (CD) Maximum recording power (CD-R, -RW) Laser diode ON (except Adjustment mode)	Pressing the REC key provides the maximum recording power condition, and lights the REC LED in green. Subsequent pressing of the REC/MUTE key with the CD setting lights the REC LED in amber, and outputs the playback power. With CD-R or CD-RW setting, the REC LED lights in red and the maximum recording power is output by normal EFM. If you cancel the maximum recording power with the CD-R or CD-RW setting by pressing the STOP key, the setting automatically returns to that for a CD. **Caution:** The laser diode may be damaged if you press the key before adjustment. For PDR-509, when the REC MUTE key is pushed, the REC LED lights red, even if the REC key is pushed, the REC LED does not light.

Adjustment modes (with the INPUT selector set to OPTICAL (OPT))

Key Name	Operation in Test mode	Descriptions
DISPLAY OFF		To turn on/off the DISP_OFF LED.
MANUAL WRITE		To turn on/off the [MANUAL] LED.
ERASE	To specify the type of disc.	To switches the servos in accordance with the specified disc. The key input cyclically switches in the sequence of CD →CD-R →CD-RW. The disc segments on the FL display are then lit. Switching is enabled only in STOP state.
INPUT SELECTOR SW	To select the adjustment modes.	When the INPUT selector is not set to ANALOG, the ALC segments light, and the following adjustments are enabled: Be sure to return the selector to ANALOG when no adjustment is made.
AUTO/MANUAL	To select the adjustment modes. To turn off all the FL indications.	When the INPUT selector is not set to ANALOG, the above adjustment modes can be selected. Pressing the key with the INPUT selector set to ANALOG turns off all the FL indications for about 5 seconds.
REC For PDR-509, JOGDIAL Counterclockwise	To change the adjustment value in the minus direction	The adjustment value is changed in the minus direction and displayed.
REC/MUTE For PDR-509, JOGDIAL Clockwise	To change the adjustment value in the plus direction	The adjustment value is changed in the plus direction and displayed.
SKIP SET For PDR-509, JOGDIAL	To register the adjusted value.	The adjusted value is registered. When backup is correctly completed, the "?" segments will go dark.
SKIP CLEAR	To direct the track balancing process. To initialize the adjustment value.	The 32 segments (sampling display) light for a moment upon key input, and the tracking balance process is executed. This key operation must be made after FOCUS ON and SPINDLE ON. When the key is held pressed for 4 seconds, the adjustment value is initialized. When the backup is correctly completed, the "?" segments will go dark.
SYNC (remote control: RANDOM)	To direct the averaging process.	The 48 segments light upon key input, and the averaging process is executed. This key operation must be made in STOP state after specifying the type of disc.

Modes other than adjustment mode (with the INPUT selector set to ANALOG)

Key Name	Operation in Test mode	Descriptions
DISPLAY OFF		To turn on/off the DISP_OFF LED.
MANUAL WRITE		To turn on/off the [MANUAL] LED.
ERASE	To specify the type of disc	To switches the servos in accordance with the specified disc. The key input cyclically switches in the sequence of CD →CD-R →CD-RW. The disc segments on the FL display are then lit. Switching is enabled only in STOP state.
AUTO/MANUAL	To select the adjustment modes. To turn off all the FL indications.	When the INPUT selector is not set to ANALOG, the above adjustment modes can be selected. Pressing the key with the INPUT selector set to ANALOG turns off all the FL indications for about 5 seconds.
REC		Used for outputting the maximum recording power.
REC/MUTE		Used for outputting the maximum recording power.
SKIP ON/OFF For PDR-509, TIME	To switch the displayed time	To turn on/off the SKIP segments. When the SKIP segments are on, the absolute time of a disc is displayed. When the SKIP segments are off, the elapsed Q-data time of each track of a disc is displayed.
SYNC (remote control: RANDOM)	To direct the averaging process	The 48 segments light upon key input, and the averaging process is executed. This key operation must be made in STOP state after specifying the type of disc.

Caution: Each servo operates independently in Test mode. So, for disc playback, you have to operate the keys by the correct procedure and sequentially close the servos.

[Playing a disc in Test mode]

Operate the keys in the following sequence to play a disc.

FINALIZE	Lights the laser diode and closes the focus servo.(The PGM key is also valid.)
↓	
PLAY	Starts up the spindle motor and closes the spindle servo.
↓	
PAUSE	Closes the tracking servo.

Operate the keys in a 2- to 3-second intervals

[Switching the time display in Test mode]

When the INPUT selector is set to ANALOG, you can change the time display with tracking on by pressing the SKIP ON/OFF key.
SKIP OFF (SKIP segments lit) : Absolute time (ATIME)
SKIP ON (SKIP segments unlit) : Sub Q TIME
For PDR-509, this key becomes TIME Key.

[Operation for line adjustment in Test mode]

Operating procedure:

① Set to Test mode after setting the INPUT selector to ANALOG.
② Make preparations for measurements.
③ Set the INPUT selector to OPTICAL (OPT) or COAXIL (COAX). (The ALC segments light.)
④ Select the adjustment items with the AUTO/MANUAL key.

You can select the adjustment items for steps ③ and ④ in the combinations listed below.
After operation of steps ③ and ④, the adjustment item number is displayed at TNO of the FL display, and the current set value of that item is displayed at MIN and SEC.

⑤ Press the REC key to change the value to the minus direction or the REC MUTE key to change it in the plus direction.
(For PDR-509, the value changes into the direction of the plus if JOGDIAL turns clockwise. The value changes into the direction of the minus if JOGDIAL turns counterclockwise.)
You may see the Q data or ATIP data of the disc by switching the INPUT selector to ANALOG in this state. If you set the INPUT selector back to OPTICAL (OPT) again, the former adjustment item is resumed.

⑥ When the desired value is set, register it by pressing the SET key.
The registered value lights and the "?" segments go dark when the backup of the value in EEPROM is completed.

⑦ If you wish to initialize adjustment values 1 to 4 to the default values of the microcomputer, press and hold the SKIP CLEAR key for about 4 seconds with the INPUT selector set to OPTICAL (OPT) or COAXIL (COAX). Adjustment values 1 to 4 are initialized and registered in EEPROM.

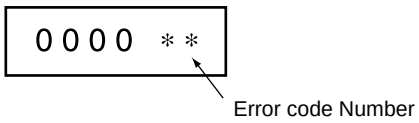
11. ERROR CODES

11.1 ERROR CODE DISPLAY FOR SERVICE

With PDR-555RW, PDR-19RW, PDR-V500:

The PDR-555RW, PDR-19RW, and PDR-V500 can display error codes for service.
When the STOP key is held down for about 5 seconds in stop state in Normal mode, an FL display as shown below is obtained.

● Display



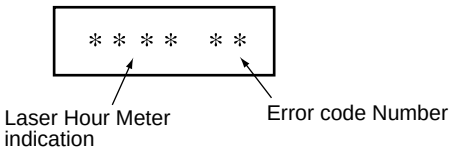
An error code for service is displayed in the right two FL digits.

The error code for service is displayed as a number (ERROR NUMBER), which follows a message "CHECK DISC" or "CHECK." For details, see the table below.

With PDR-509

Laser Hour Meter Indication and Error Code Display for Service
The PDR-509 can display the total turn-on time of the laser diode and error codes for service.
When the STOP key is held down for about 5 seconds in stop state in Normal mode, an FL display as shown below is obtained.

● Display



Left 4 FL digits : Total turn-on time of the laser diode
Right 2 FL digits : Error code for service

The total turn-on time of the laser diode is displayed in the range of 0 to 5100.
The error code for service is displayed as a number (ERROR NUMBER), which follows a message "CHECK DISC" or "CHECK." For details, see the table below.
To initialize the total turn-on time of the laser diode, hold STOP key down for about 5 seconds in stop state with the INPUT selector set to ANALOG in Test mode.
The message "CLEAR" is displayed, and the total time is cleared.

Error code table for service

Code	Symptom	Contents of Error	Possible Cause	Checkpoints
H0	No operation even when power is supplied.	Communication between mechanism controller and mode controller is not achieved.	• Improper soldering • Pattern short	IC204 (PD4956) IC205 (PDJ014) For PDR-509, IC301 (PE5109A) IC351 (PDJ014)
H1	(CHECK display)	Defective mechanism controller terminals	• Short-circuiting of parts • Improper power supply	IC203 (HD74HC573) For PDR-509, IC371 (HD74HC573)
H2	Pre-recording process does not complete, and the tray does not open. (CHECK display)	Improper input voltage at the mechanism-control terminals (pins 22, 23, 24)		IC247(PA9004) For PDR-509, IC201(PA9007)
H5	Pre-recording process disabled (CHECK display)	Improper IC705 data writing	• Defect in IC705 For PDR-509, IC303	IC705 (PYY1196) for PDR-509, IC303 (PYY1196)
L＊	The unit stops during the tray open/close operation. (CHECK display)	Improper loading	• Defective tray position sensor • Defective loading motor • Improper soldering • Pattern short • Improper power supply	IC352 (BA5932) for PDR-509, IC451 (M56788)
E＊	The unit stops when PLAY or REC/PAUSE starts. (CHECK display)	Defective slider • The pickup cannot be returned to the specified position.	• Disconnected flexible cable • Defective drive circuit • Abnormal power supply • Abnormal TOC position switch • Improper soldering	S601 (MPU10230) IC352 (BA5932) IC353 (CXD2585Q) for PDR-509, S601 (MPU10230) IC451 (M56788) IC401 (CXD2585Q)
P＊	The unit does not read the inserted disc, and stops. (CHECK DISC display)	Defect in spindle • Disc upside-down. • Dirty or cracked disc • Abnormal disc rotation • No signal obtained from the disc	• Defective spindle motor • Defective spindle drive circuit • Abnormal FG signals • Defective WBL circuit • Defective decoder circuit • Unable to read ATIP or subcode • High error rate	PC651 (NJL5803K) IC352 (BA5932) IC353 (CXD2585Q) for PDR-509, PC651 (NJL5803K) IC451 (M56788) IC401 (CXD2585Q)

Code	Symptom	Contents of Error	Possible Cause	Checkpoints
C∗	The unit stops before it enters REC/PAUSE mode.	Defects related to the recording laser power • Dirty or cracked disc • The optimum recording power cannot be obtained. • Trouble in RF detection.	• Defective laser diode • Trouble in RF detection • Defective RFT RFB circuit • Recording power is not sufficient. • Improper soldering, pattern short • Trouble with power supply • Unable to read ATIP or subcode	IC247 (PA9004) IC103 (AK8563) IC208 (TC7S04) IC209 (TC7S14) for PDR-509, IC201 (PA9007) IC101 (AK8563) IC363 (TC7S04) IC364 (TC7S14)
F∗	The unit stops during playback or recording.	Defective pickup • Unable to focus because of dirt or crack on the inserted disc. • Unable to output the proper laser power	• Defective laser diode • Defective focus drive circuits • Defective pickup • Improper soldering • Pattern short • Trouble of power supply	IC352 (BA5932) IC353 (CXD2585Q) for PDR-509, IC451 (M56788) IC401 (CXD2585Q)
A∗	The unit stops in a recording-related operation, displaying "CHECK DISC."	• Unable to focus Stop during recording • The unit stops, being obstructed by a dirt or a crack on the disc.	If any hardware trouble occurs before displaying A∗ or d∗, the unit stops displaying a code other than these codes. Therefore, these service codes are generated only for troubles with the disc.	
d∗	The unit stops in a recording related operation, displaying "CHECK DISC." The unit does not read the inserted disc, and stops.			

The indication for ∗ shows the mechanism mode listed below:

No.	Mechanism Mode	No.	Mechanism Mode	No.	Mechanism Mode
0	PLAY	5	SETUP	A	REC
1	OPEN	6	TOC READ	B	TOC REC
2	STOP	7	–	C	OPC
3	–	8	SEARCH	D	TOC CHECK
4	–	9	REC/PAUSE	E	PMA, ACTUAL PAUSE REC

Initializing the Error Code Display

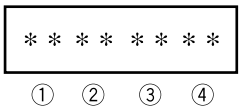
To clear the error codes, hold the "MENU" key down for about 10 seconds in Normal mode.

11.2 ABOUT FULL ERROR CODES

With the PDR-555RW, PDR-19RW, and PDR-V500, a full error code is displayed on the FL display when you press the SKIP PLAY key and MENU key simultaneously.
The full error codes are not backed up, and are cleared when the power is turned off.
With the PDR-509, press the TIME and DISP OFF keys simultaneously.

● Display

The eight digits are displayed as shown below:



The values of each 2 digits for ① to ④ (8 digits in total) are shown below:

Two digits displayed for ① : The lower digit shows the operation when the error is detected.

×0 : Unknown
×1 : Tray open
×2 : Tray close or open
×3 : SETUP (starting up a disc)
×4 : TOC, PMA read (including SETUP)
×5 : PLAY
×6 : SEARCH
×7 : REC/PAUSE
×8 : REC
×9 : LEAD OUT REC
×A : TOC REC
×B : PMA REC
×C : Power calibration
×D : TOC CHECK
×E : ACTUAL PAUSE REC
×F : Unknown

When "F1" is displayed in two digits for ②, the digits for ① show the number of the defective pin of the mechanism control.

Two digits displayed for ② : Error Mode

Errors Generated in the Mechanism Control

Mode No. : Mode Name
00 : Unfixed mode (inner condition unknown, upon hardware reset)
01 : Invalid mode
02 : STOP
03 : Laser diode on (playback power)
04 : Focus ON
05 : Spindle ON
06 : Tracking ON
07 : Direct sequence forward 1-track jump using DIRC
08 : Direct sequence reverse 1-track jump using DIRC
09 : Direct sequence forward 1-track jump repeat using DIRC
10 : Direct sequence reverse 1-track jump repeat using DIRC
11 : Auto sequence 10-track forward jump repeat
12 : Auto sequence 10-track reverse jump repeat
13 : Auto sequence 50-track forward jump repeat
14 : Auto sequence 50-track reverse jump repeat
15 : Auto sequence forward M-track movement
16 : Auto sequence reverse M-track movement
17 : PAUSE
18 : PLAY
19 : Seek track 0
20 : Blank search
21 : REC
22 : REC to PAUSE (REC END)
23 : ATIP TIME search
24 : Q-code TIME search
25 : Q-code track search
26 : Forward 300-track movement
27 : Reverse 300-track movement
30 : TOC area search
31 : Tray open
32 : Tray close
33 : Setup (→ PLAY)
34 : TOC read
35 : PLAY normal
36 : Search → PLAY
37 : REC. PAUSE
39 : Lead-out REC
40 : TOC (lead-in) REC
41 : PMA REC
42 : PCA REC
43 : TOC check
44 : Actual REC PAUSE
45 : Initializing
47 : 2-track jump setting in pause mode
48 : 1-track jump setting in pause mode
51 : Search → PAUSE
52 : PMA read
53 : Laser diode nominal recording power output
54 : Searching area with Q code
57 : Laser diode maximum recording power output
58 : Laser diode recording power continuous sweep mode
59 : Slider forward movement
60 : Slider reverse movement
61 : Calculating the track pitch and the line velocity of the disc by measuring T0 and T1.
62 : Auto sequence 1-track forward jump
63 : Auto sequence 1-track reverse jump

64 : Auto sequence 1-track forward jump repeat
65 : Auto sequence 1-track reverse jump repeat
66 : Auto sequence 10-track forward jump
67 : Auto sequence 10-track reverse jump
68 : (Sound-generating) Scan mode using auto sequence 10-track forward jump.
69 : (Sound-generating) Scan mode using auto sequence 10-track reverse jump.
70 : Auto sequence 50-track forward jump
71 : Auto sequence 50-track reverse jump
72 : High-speed scan mode using auto sequence 50-track forward jump.
73 : High-speed scan mode using auto sequence 50-track reverse jump.
74 : Several forward jumps in DTRNUM by combining auto sequence 2N-track jumps
75 : Several reverse jumps in DTRNUM by combining auto sequence 2N-track jumps
76 : REC mode continuous operation after resuming from a power failure
78 : Blank search
79 : Resume mode from "tracing error" and "out of focus" during REC

Errors the Mode Control Generates

Mode No. : Mode Name
91 : Loading error

C7 : Cannot enter REC/PAUSE of power calibration even when 60 seconds elapsed.

d0 : Stops owing to a resume failure or STOP key input.
d4 : Insufficient data in TOC PMA read
d7 : RF check failure at REC/PAUSE
db : PMA REC does not finish even when 60 seconds have elapsed
dd : Stops owing to a TOC check error or STOP key input
df : Cannot enter REC/PAUSE even when 60 seconds have elapsed, cannot start REC even when 10 seconds have elapsed, or resuming from tracing error does not complete even when 60 seconds have elapsed

F0 : Communication error of the mechanism control
F1 : Hardware error of the mechanism control: The number of the defective pin of the mechanical control is displayed at TRACK.
F2 : A/D input (RFT, RFB) error of the mechanism control
F5 : RID serial number error

Two digits displayed for ③ : Recording submode when the error was generated

10 : While setting REC/PAUSE
20 : During REC/PAUSE
30 : During REC
40 : While stopping REC
50 : Unlocking, during SCMS stop

Two digits displayed for ④ : Other condition when the error was generated is displayed by a HEX code

bit 7 : Out of focus
bit 6 : Sync loss detected during REC
bit 5 : tracing error during REC
bit 4 : TOC read error (insufficient data)
bit 3 : Improper A/D value of RFT, RFB
bit 2 : No meanings
bit 1 : No meanings
bit 0 : No meanings